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VERTICAL ORGANIC FIELD-EFFECT TRANSISTORS

- ON THE UNDERSTANDING OF A NOVEL DEVICE CONCEPT -

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Diese Arbeit ist dem Mann gewidmet, der mich mit seiner Begeisterung für die Physik mehr als jeder andere inspiriert hat: meinem Vater.

ZUSAMMENFASSUNG

Diese Arbeit stellt eine eingehende Studie des sogenannten Vertikalen Organischen Feld-Effekt-Transistors (VOFET) dar, einer neuen Transistor-Geometrie, welche dem stetig wachsenden Bereich der organischen Elektronik entspringt. Dieses neuartige Bauteil hat bereits bewiesen, dass es in der Lage ist, eine der fundamentalen Einschränkungen herkömmlicher organischer Feld-Effekt-Transistoren (OFETs) zu überwinden: Die für Schaltfrequenz und An-Strom wichtige Kanallänge des Transistors kann im VOFET stark reduziert werden, ohne dass teure und komplexe Strukturierungsmethoden genutzt werden müssen. Das genaue Funktionsprinzip des VOFET ist bisher jedoch weitgehend unerforscht. Durch den Vergleich von experimentellen Daten mit Simulationsdaten des erwarteten Bauteil-Verhaltens wird hier ein erstes, grundlegendes Verständnis des VOFETs erarbeitet. Die so gewonnenen Erkenntnisse werden im Folgenden genutzt, um bestimmte Parameter des VOFETs kontrolliert zu manipulieren. So wird beispielsweise gezeigt, dass die Morphologie des organischen Halbleiters, und damit seine Abscheidungsparameter, sowohl für die VOFET-Herstellung als auch für den Ladungsträgertransport im fertigen Bauteil eine wichtige Rolle spielen. Weiterhin wird gezeigt, dass der VOFET, genau wie der konventionelle OFET, durch das Einbringen von Kontaktdotierung deutlich verbessert werden kann. Mit Hilfe dieser Ergebnisse kann gezeigt werden, dass das Funktionsprinzip des VOFETs mit dem eines konventionellen OFETs nahezu identisch ist, wenn man von geringen Abweichungen aufgrund der unterschiedlichen Geometrien absieht. Basierend auf dieser Erkenntnis wird schließlich ein VOFET präsentiert, welcher im Inversionsmodus betrieben werden kann und so die Lücke zur konventionellen MOSFET-Technologie schließt. Dieser Inversions-VOFET stellt folglich einen vielversprechenden Ansatz für leistungsfähige organische Transistoren dar, welche als Grundbausteine für komplexe Elektronikanwendungen auf flexiblen Substraten genutzt werden können.

ABSTRACT

This work represents a comprehensive study of the so-called vertical organic field-effect transistor (VOFET), a novel transistor geometry originating from the fast-growing field of organic electronics. This device has already demonstrated its potential to overcome one of the fundamental limitations met in conventional organic transistor architectures (OFETs): In the VOFET, it is possible to reduce the channel length and thus increase On-state current and switching frequency without using expensive and complex structuring methods. Yet the VOFET's operational principles are presently not understood in full detail. By simulating the expected device behaviour and correlating it with experimental findings, a basic understanding of the charge transport in VOFETs is established and this knowledge is subsequently applied in order to manipulate certain parameters and materials in the VOFET. In particular, it is found that the morphology, and thus the deposition parameters, of the organic semiconductor play an important role, both for a successful VOFET fabrication and for the charge transport in the finished device. Furthermore, it is shown that VOFETs, just like their conventional counterparts, are greatly improved by the application of contact doping. This result, in turn, is used to demonstrate that the VOFET essentially works in almost exactly the same way as a conventional OFET, with only minor changes due to the altered contact arrangement. Working from this realisation, a vertical organic transistor is developed which operates in the inversion regime, thus closing the gap to conventional MOSFET technology and providing a truly promising candidate for high-performance organic transistors as the building blocks for advanced, flexible electronics applications.

CONTENTS

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INTRODUCTION

This thesis, just like many other PhD theses and indeed most documents today, was written on a modern computer. This computer contains a whole variety of electronic components, most of which have been developed in the last 200 years and are still the subject of continuous improvement and downscaling. The most common of these components is the transistor. This device forms the basis of all modern technology. In fact, life as we know it today would not have been possible without the invention of the transistor. The Austrian physicist Julius Edgar Lilienfeld was the first to propose a device concept which utilises electric fields to change the electrical conductivity of a given material so as to amplify a current signal between two contacts by use of a third contact [1]. This concept would later be termed the *field-effect transistor* (FET). The first solid-state transistor was realised experimentally in 1948 by the Americans and later Nobel Prize winners William Shockley, Thomas Bardeen and Walter Brattain at Bell Laboratories in the form of the bipolar junction transistor (BJT) [2]. The subsequent story of the transistor is one of tremendous success. Among the different device concepts presented in later years, the most successful one by far was the metal-oxide-semiconductor field-effect transistor (MOSFET), which was first realised by Kahng and Atalla in 1960 [3]. MOSFET technology today is the essential building block for virtually all logic circuits and electronics devices, whether they are as simple as a digital alarm clock or as advanced as a super-computer. While MOSFETs are based largely on the inorganic semiconductor silicon, one of the most abundant elements on this planet, recent developments provide an entirely new and exciting development: the prospect of flexible electronics devices made from organic semiconductor materials.

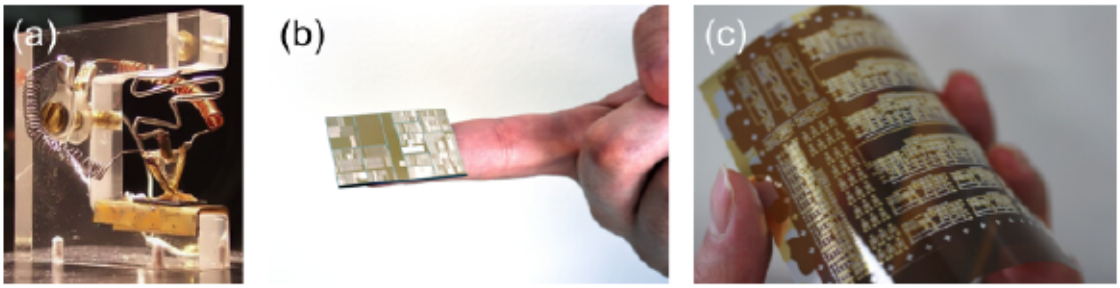

Figure 0.1.: The evolution of transistors: (a) Reconstruction of the original point-contact transistor developed by Shockley, Bardeen and Brattain; (b) first lab demonstrator of IBM's latest 7 nm channel MOSFET; (c) lab demonstrator of OFETs on flexible substrates. Images taken from ref. [4–6].

Organic semiconductors have been the topic of research since the 1960s, but it was mainly the discovery of efficient electroluminescence in organic diode structures in the late 1980s which caused the continuously growing commercial interest in organic electronics [7]. Due to large efforts both in the development of new materials and device architectures, the field of organic electronics has already produced several market applications, not least among them organic light-emitting diodes (OLEDs) and organic photovoltaic cells (OPVs). What sets organic semiconductors apart from their inorganic counterparts is the way in which these materials can be produced and manufactured into electronics devices: Conventional semiconductors, such as silicon, require manufacturing processes that imply chemicals which are often harmful to the environment. Furthermore, while silicon is one of the most abundant materials on earth, it rarely occurs in a pure form and has to be harvested and cleaned by complex and expensive procedures. Organic semiconductors, on the other hand, can be synthesised in a lab, the chemical and physical properties of a given material can even be altered to tailor it to the specific needs of a certain application. Furthermore, organic semiconductors can be processed in several different, inexpensive ways, which may be more environmentally friendly and allow for fabrication of devices on flexible substrates, as shown in figure 0.1. Organic semiconductors therefore open up entirely new possibilities for advanced and flexible consumer electronics and it is to be expected that organic electronics will become a multi-billion dollar market. The foundation for this has already been set by OLED displays in mobile phones and TVs, which already have an annual market share of approximately 10B$. However, the largest market share in the years to come will go to organic logic circuitry and memory devices, as such technology is required to realise any form of advanced, flexible electronics product.

The aim and focus of this thesis therefore is the combination of the two technologies detailed above: the combination of MOSFET technology and organic semiconductors - in short, the organic field-effect transistor (OFET) and in particular the novel architecture of vertical organic field-effect transistors (VOFETs). While conventional OFETs have been researched for quite some time [8], the novel VOFET architecture has only been developed recently and is at present not very well understood.

In chapter 1 of this thesis, the concept of organic semiconductors, as well as their fundamental properties, will be introduced. As a pre-requisite to the device investigated in this thesis, the conventional OFET will be discussed in chapter 2 and, building on this

discussion, chapter 3 will introduce the novel VOFET architecture, explain its theoretical superiority to the conventional OFET and also discuss other vertical transistor geometries. Chapter 4 contains a detailed explanation of the experimental methods used during the work that lead to this thesis. It further gives information on the materials used for sample fabrication. In the following chapters, the research results leading to this thesis will be presented, starting with chapter 5, which discusses some basic material optimisation results. Chapter 6 is dedicated to the fundamental understanding of the VOFET's operational principles. Here, the charge transport through the device is discussed in more detail and first conclusions on the basic operational principle of the VOFET are drawn, supported by results from both experiment and simulation. Chapter 7 continues this discussion by introducing the concept of molecular doping as a tool to understand the VOFET operation. It demonstrates the great potential of selective contact doping as a method for improving device performance and concludes with a very important realisation concerning the limitations of the VOFET. Building on all these results, chapter 8 presents what is possibly the world's first vertical organic inversion mode transistor, a device which truly combines the operational principle of a silicon MOSFET with the design freedom of organic semiconductors. Chapter 9 summarises once again the results presented in the previous chapters and aims to provide a brief outlook for future work on this fascinating technology.

BASIC PRINCIPLES OF ORGANIC SEMICONDUCTORS AND RELATED DEVICES

1. THE PHYSICS OF ORGANIC SEMICONDUCTORS

This chapter introduces the most fundamental concepts involved in organic semiconductor physics. Starting with a first principles derivation of the special nature of certain organic molecules, the formation of organic solids will be discussed, as well as their electrical and structural properties. For the special case of organic semiconductors, the concept of quasi-particles will be introduced and potential transport mechanisms of such particles will be discussed. In the last section, the concept of molecular doping for organic materials will be introduced as an important tool for device optimisation.

In the broadest sense, the term *organic semiconductor* refers to a material which comes from the area of *organic chemistry* and possesses classical semiconducting properties. Put more specifically, an organic semiconductor is a material whose structure is based largely on hydrocarbons (often in the form of benzene rings, compare figure 1.1) and whose electrical conductivity may be increased beyond the typical insulator level (approximately $10^{-10}(\Omega cm)^{-1}$) by certain processes, e.g. doping, heating or illumination. Elements such as fluorine, nitrogen, oxygen, sulphur or certain metals are often incorporated into these hydrocarbon structures in order to adapt their properties for specific applications.

One generally differentiates between polymer semiconductors, i.e. macromolecules which are made of many repeating units of hydrocarbon-based monomers and may be several hundred nanometers long, and so-called *small molecules*, which - as the name suggests - are considerably smaller in size and have either no repeating units at all or only a very limited number of such units (these are referred to as oligomers). Semiconducting materials made purely of carbon, such as fullerenes or carbon nanotubes, also fall under the definition of organic semiconductors. A few examples of typical organic semiconductors are shown in figure 1.1, together with their chemical structures.

As is visible already from these few examples, another definition of the sub-categories of organic semiconductors may be derived simply from the form in which they most often occur: Most small molecules fall under the definition of organic solids [9], that is to say, they naturally form single-crystalline, polycrystalline or amorphous solids. These are generally processed by thermal evaporation under vacuum, as will be explained further in chapter 4. Larger molecules, and in particular many polymers, are better described as organic soft matter and are typically processed from solution as they would decompose during the thermal evaporation process.

The remainder of this chapter will focus on small molecule semiconductors, including also the class of fullerenes. As polymer semiconductors played no part in the work leading to this thesis, they shall not be discussed further, although many of the most fundamental concepts of organic semiconductors are the same for polymers and small molecules. For more detailed information on the material class of polymer semiconductors, the interested reader is referred to standard textbooks such as ref. [10] and [11].

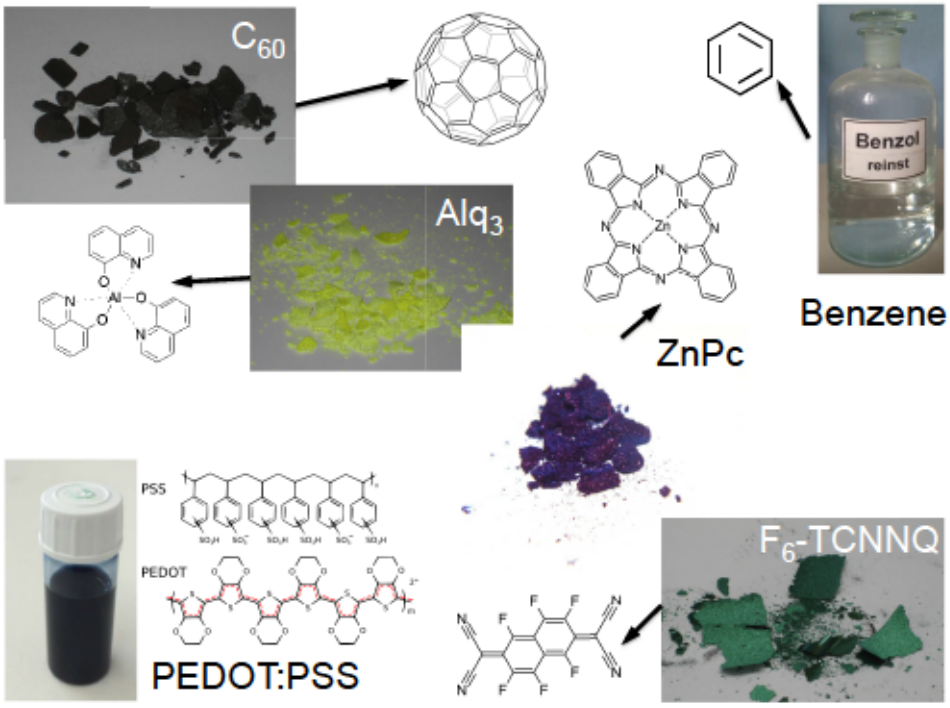

Figure 1.1.: Examples of organic compounds: The basic building block benzene (top right); the buckminster fullerene (C_{60}, top left), which is a common n-type semiconductor and absorber; the n-type semiconductor and emitter tris(8hydroxyquinolinato)aluminium (Alq_3, left); the p-type semiconductor zinc phthalocyanine (ZnPc, right), the p-dopant 2,2'(perfluoronaphthalene2,6diylidene)dimalononitrile (F_6-TCNNQ, bottom right) and the polymer semiconductor PEDOT:PSS in solution (bottom left). All images by IAPP.

1.1. ELECTRONIC AND STRUCTURAL PROPERTIES OF ORGANIC SEMICONDUCTORS

In classical solid-state physics, the electronic properties of e.g. a semiconductor are typically derived through two different paths: Either one uses a macroscopic approach such as the Kronig-Penney model, which derives the material's band structure from the periodic potential of the entire crystal lattice using Bloch's theorem, or a microscopic approach such as the tight-binding approximation, where the band structure of the solid is extrapolated from the wave function overlaps of two nearest neighbours in the crystal [12]. Both methods lead to a clearly defined band structure of the material under investigation. For a semiconductor, such as Si, this yields clearly defined valence and conduction bands, with the Fermi level inside the energy gap between those two bands. For the case of organic semiconductors, the determination of the energy levels relevant for transport

is somewhat more complex owing to the complexity of the molecules themselves. In order to understand the fundamental nature of organic semiconducting compounds, one therefore needs to first understand the nature of intra-molecular bonds.

1.1.1. INTRA-MOLECULAR BONDS AND ENERGY LEVELS

One can illustrate the basic principles of energy level formation and intra-molecular bonds by the simple construct of the ionised hydrogen molecule[1]: Assuming a molecule with two hydrogen atoms A and B and a single electron shared between them, the total wave function of the system will have the form $\Psi = \Psi(\vec{R}_A,\vec{R}_B,\vec{r})$ and obeys the Schrödinger equation, such that

$$\hat{H}\Psi = \hat{H}_r\Psi + \hat{H}_{\vec{R}_A}\Psi + \hat{H}_{\vec{R}_B}\Psi = E\Psi \tag{1.1}$$

where $\vec{R}_A$ and $\vec{R}_B$ are the position vectors of the two hydrogen nuclei and $\vec{r}$ represents the position vector of the electron. This analytically unsolvable expression[2] can be simplified by the Born-Oppenheimer approximation [14], where it is assumed that the motion of the nuclei is significantly slower than that of the electron, owing to the great difference in masses. Following this approach, the wave function can be expressed as $\Psi(\vec{R}_A, \vec{R}_B, \vec{r}) = \Psi(\vec{R}_A, \vec{R}_B)\Psi(\vec{r})$, so that equ. 1.1 can be simplified to

$$\hat{H}\Psi = \hat{H}^{elec}\Psi(\vec{r}) + \hat{H}^{vibr}\Psi(\vec{R}_A, \vec{R}_B) = E^{elec}\Psi(\vec{r}) + E^{vibr}\Psi(\vec{R}_A, \vec{R}_B) \tag{1.2}$$

which is now separated into an electronic and a vibronic part. The electronic part can be solved analytically by use of the linear combination of atomic orbitals (LCAO) method to yield

$$\Psi(\vec{r}) = c_A\Psi_A + c_B\Psi_B \tag{1.3}$$

where Ψ_A and Ψ_B are the atomic wave functions of the hydrogen atoms (for example of the *1s* orbitals) and c_A and c_B are the respective expansion coefficients. These have the allowed solutions $c_A = \pm c_B$ and thus define the symmetric and anti-symmetric molecular wave functions, denoted as Ψ_+ and Ψ_-. The energy eigenvalues related to these wave

[1] For a basic, but excellent discussion of the ionised hydrogen molecule and its implications for the benzene ring and electronic movement in a crystal lattice, the interested reader is also referred to chapters 10 and 13 of ref. [13]

[2] The Hamiltonians in equ. 1.1 contain both the kinetic and potential energies of the nuclei and the electron. Since these are not independent for the individual components, an analytic solution for Ψ cannot be found.

functions represent the energies of a bonding and anti-bonding state of the hydrogen molecule and thus result in two distinct energy levels with an energy gap in-between, as shown in figure 1.2. In a typical organic compound, the situation is naturally much more complex, owing to the presence of several atoms with considerably more than just one electron. Here, more involved methods, e.g. density functional theory (DFT), have to be employed to obtain the electronic structure of the system.

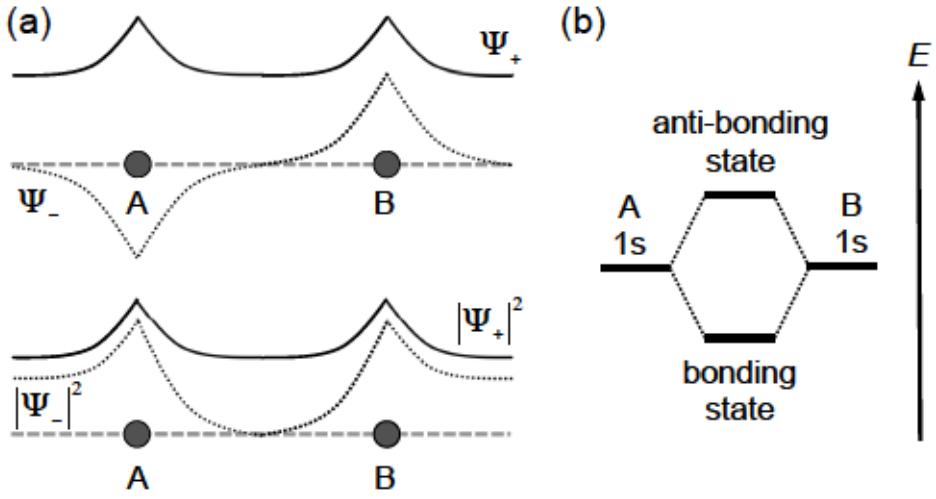

Figure 1.2.: (a) Schematic representation of the bonding and anti-bonding wave functions in a hydrogen molecule with hydrogen atoms at positions A and B. (b) Energy level diagram of the ionised hydrogen molecule as given by the energy eigenvalues of the wave functions depicted in (a).

What sets organic semiconductors apart from other organic compounds is the fact that they possess so-called *conjugated π-systems*. This term refers to a special set of delocalised electrons occurring in certain organic molecule configurations, such as the benzene ring. Carbon atoms in a benzene ring are covalently bound to one another and to one hydrogen atom per carbon atom, as shown in figure 1.3 (a). The bonds in this case are provided by the so-called *sp^2-hybridisation,* i.e. by a mixing of the *2s* and *$2p_{x,y}$* orbitals of the respective carbon atoms. The majority of electrons present in the benzene ring are bound in these hybrid orbitals and thus form the covalent σ-bonds of the benzene ring (with binding energies of 1 - 7 eV and bond lengths of 0.1 - 0.3 nm [9]). A small number of electrons, however, remains in the *$2p_z$*-orbitals, which orientate perpendicularly to the ring-plane. These electrons are delocalised with respect to the carbon atoms and form the so-called π-bonds. It is this delocalisation of a small number of electrons with respect to the molecule which gives certain organic compounds their semiconducting properties.

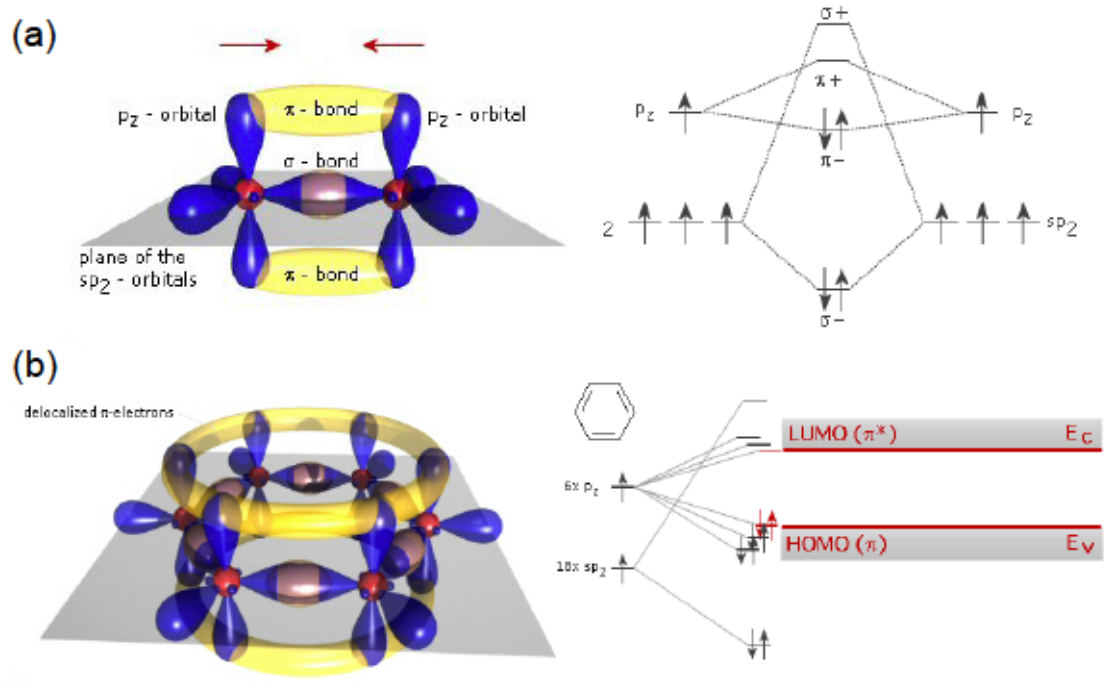

Figure 1.3.: (a) Schematic representation of an ethene molecule with its sp_2hybridisation orbitals forming σ-bonds and p_z-orbitals forming π-bonds. Related energy diagrams are shown on the right. (b) A benzene ring with delocalised π-electrons shown as yellow rings above and below the carbon atom plane. HOMO and LUMO formation is shown on the right. Figures taken from ref. [15].

In analogy to the conduction and valence band known in classical semiconductors, the π-bonds provide a series of energy levels. The highest occupied molecular orbital (HOMO) is equivalent in this picture to the valence band, whereas the lowest unoccupied molecular orbital (LUMO) is equivalent to the conduction band. The size of the energy gap between these two states depends largely on the spatial extend of the conjugated π-system: The more extended the π-system, the smaller the bandgap of the organic semiconductor. According to Koopmans' theorem [16], it is further possible to relate HOMO and LUMO to the experimental quantities of ionisation potential (IP) and electron affinity (EA).

So far, the properties of single organic molecules have been considered and the formation of intra-molecular bonds and energy levels has been explained. In the next paragraph, the inter-molecular forces leading to the formation of organic solids will briefly be discussed.

1.1.2. INTER-MOLECULAR BONDS AND THE FORMATION OF ORGANIC SOLIDS

Since an organic solid consists of many molecules, which are placed in direct vicinity of each other, it is obvious that some of the properties derived for single molecules may change when observing a macroscopic system of these same molecules. Indeed, the

HOMO and LUMO determined for an organic solid differ from those of individual molecules in the gas phase [17]. In this context, the afore-mentioned approximation of the HOMO and LUMO by the ionisation potential and electron affinity seems considerably more sensible and is therefore used to determine the HOMO and LUMO of real organic solids experimentally (e.g. by ultraviolet photon spectroscopy, UPS).

The individual molecules of an organic solid are held together by the weak van der Waals forces (binding energy approx. 100 meV). These forces, like the formation of the HOMO and LUMO states, are a result of the delocalised π-electrons: Due to fluctuations in the electron distribution, a temporary dipole can form on a specific molecule, which may temporarily polarise the molecules surrounding it. This leads to Coulomb attractions which are weak and short-lived, yet sufficient to bind individual molecules to one another to form an organic solid. Polar organic molecules are further bound together by the much stronger permanent dipole interaction.

For a more extensive discussion of the inter-molecular bonds of organic semiconductors, the interested reader is referred to ref. [9]. Suffice it to say for the purpose of this thesis that the strength of these inter-molecular bonds determines macroscopic properties of the material, such as the melting or boiling point, which become important again in chapter 4, where thermal evaporation of organic solids is discussed further. In addition, when speaking of processing organic semiconductors, the interaction strength between organic molecules in relation to the interaction with a given substrate determines the morphology of this material.

1.1.3. STRUCTURE AND MORPHOLOGY

Organic semiconductor molecules are typically much less symmetric than their inorganic counterparts. Consequently, they often form polycrystalline or even amorphous layers during processing, and although an organic single crystal is generally easier to fabricate than its Si counterpart, fabrication methods for such single crystals are still reasonably involved and more suitable for research purposes[3] than for actual mass production. If crystallites are formed at all, they will have a monoclinic or triclinic symmetry [20] and especially the electronic properties of organic semiconductors thus depend largely on the morphology of the layer, i.e. the way in which the individual molecules stack on top

[3]There are reports of organic single crystals with excellent electronic properties (see e.g. ref. [18, 19]).

of a given substrate. The packing density is often measured by the packing coefficient C_K, introduced in 1973 by Kitaigorodskii. It provides a relationship between the unit cell volume per molecule and the molecular volume and generally ranges from 0.7 to 0.9 for small aromatic compounds such as anthracene or perylene [20]. Some examples of typical packing structures are shown in figure 1.4. The simplest way of stacking is a basic vertical stack of flat molecules, as depicted in figure 1.4 (a) for TCNQ. In a slightly altered version, this stack is somewhat tilted due to the molecules being shifted with respect to each other (compare figure 1.4 (b)). The most complex of these three examples is shown in figure 1.4 (c): This is the so-called *herringbone structure*, which originates from a variation of the tilting angle for each vertical stack.

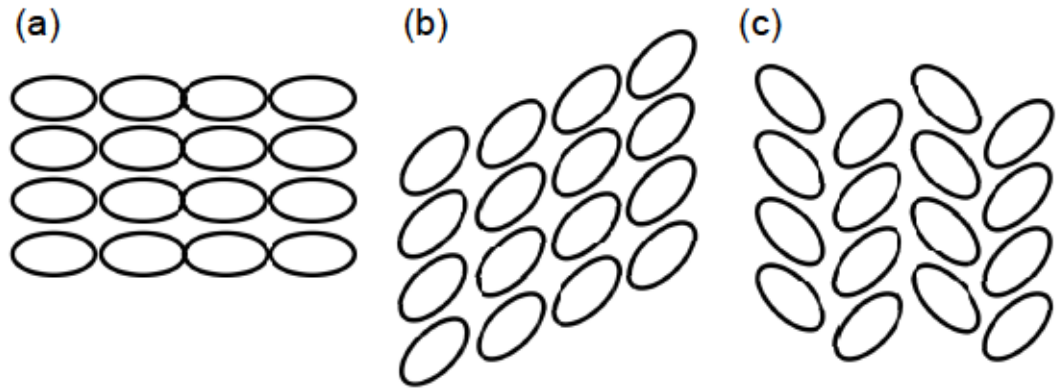

Figure 1.4.: Examples of different packing types for organic crystals: (a) simple vertical stacking, (b) tilted vertical stacking and (c) herringbone structure.

If one of the illustrated packing types is predominant in the material film and only the overall orientation of the stack is varied slightly, one speaks of a polycrystalline film, where the individual crystal domains are defined by regions of identical packing. In contrast, amorphous films are defined as films with a large variety of molecular orientations and inter-molecular distances, which may possess a certain short-range order, but are impossible to characterise by any kind of long-range order. This scenario is referred to as *spatial disorder*. In addition, amorphous materials also exhibit *energetic disorder*, which arises from the fact that the energetic environment for each molecule in the film is different due to the different arrangements of nearest neighbour effects. This energetic disorder leads to broadening of the molecular HOMO and LUMO states by a normal distribution [21].

The morphology of a layer may change due to deposition conditions, impurities or

interactions with the substrate, which all result in a change of packing density of the molecules within the solid. By introducing large disturbances of some kind, it is in fact possible to force an originally polycrystalline material into an almost amorphous growth. This will be examined further in chapter 5 of this thesis for the case of pentacene.

1.2. CHARGE CARRIER TRANSPORT

Charge carrier transport in organic semiconductors is somewhat different to the band transport of quasi-free electrons known from classical semiconductor physics. This section therefore aims to give a basic understanding of the charge transport mechanisms of organic semiconductors. It is, however, far beyond the scope of this work to discuss all theories related to this area, since charge transport in organic materials is still a matter of much discussion. A more detailed treatment of these matters can be found in textbooks and reviews, e.g. in ref. [7, 9, 22, 23].

1.2.1. QUASI-PARTICLES - POLARONS AND EXCITONS

In the previous section, it was stated that the π-electrons of a benzene ring are delocalised with respect to the atoms inside this ring and are responsible for charge carrier transport in organic semiconductors. While this general statement is true, the actual transport process is far more complex than might be expected at first glance: The π-electrons are indeed delocalised with respect to the atoms *inside* a specific benzene ring, but when considering an organic solid, these same π-electrons are tightly bound to their individual benzene rings. The organic semiconductor thus only transports charges which have been injected in some way, either by application of an external field, by illumination or by doping. These excess charges may be either positive or negative, that is to say one can inject an excess electron into the LUMO, thus forming an anion on a specific molecule, or extract an electron from the HOMO, which leaves a vacancy (hole) and forms a cation. The presence of the excess charge forces the neighbouring molecules to undergo certain relaxation processes in order to arrive at a new energetically stable state. In order to account for this phenomenon in transport theories, the concept of *polarons* was introduced. The polaron is a quasi-particle incorporating the actual charge carrier itself as well as the relaxation processes associated with it. One can distinguish three types of polarons based on the different relaxation

processes which can occur when a charge carrier moves to a specific molecule and remains there: electronic polarisation, vibronic relaxation and lattice relaxation.

Electronic polarisation of the surrounding molecules results in the formation of an *electronic polaron* and occurs on time scales of 10^{-16} s to 10^{-15} s, i.e. much faster than the typical time spent on an individual molecule by the charge carrier in question [9, 24]. *Vibronic polarons* are formed by precisely those intra-molecular vibrations in equ. 1.2 which have been excluded in the ionised hydrogen molecule by the Born-Oppenheimer approximation. These relaxation processes have a time constant of 10^{-14} s [24]. As this is approximately the same order as the average time which a charge carrier spends on a molecule, vibronic relaxations may not always be completed before the charge carrier moves to a different site. The last relaxation process is caused by phonon interactions with the charge carrier's wave function. The time scale for this process is on the order of 10^{-11} s and the interaction energy is only 0.1 to 0.3 eV, making this type of interaction virtually negligible in some materials. The presence of these polaronic effects leads to a change in energy levels of the surrounding molecules. Consequently, the HOMO and LUMO of the organic solid differ from those of a single molecule under the presence of polarons, where the magnitude of the influence depends inversely on the time constant. The total binding energy, and thus the spatial extend of the polaron, is also determined by the magnitude of each contribution. Unlike inorganic semiconductors, vibronic and lattice polaron effects play a considerable role in organic semiconductors. Thus charge carrier transport generally takes place as transport of polarons (with either holes or electrons at their centre) in these materials. For simplicity, the remainder of this work will use the terms "electron" and "hole" as being equivalent to the respective polarons, only the section concerning the different transport models will explicitly require the polaron picture once again.

Another quasi-particle associated with polaron formation is the *exciton*. This constitutes an electron-hole pair bound by Coulomb interaction and occurs most often during illumination of a semiconductor (both organic and inorganic), where photon absorption leads to excitation of electrons into higher orbitals. Other routes to exciton formation are the capture of free carriers (as happens for example in the emission layers of OLEDs) or electrical doping. The polarisation of the surrounding material causes the formation of an energetically favourable bound state of the electron and resultant hole and thus leads to an electrically neutral quasi-particle which is able to move through the solid. The exact

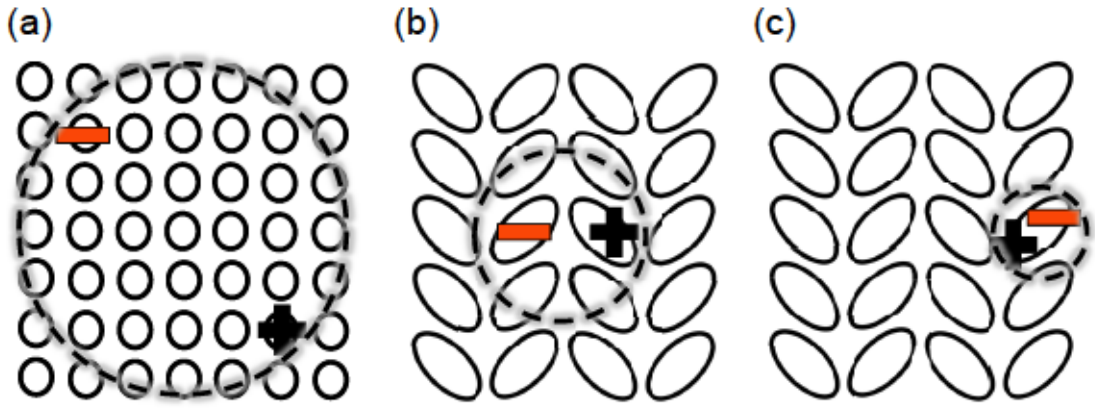

Figure 1.5.: Schematic representation of the three types of excitons: (a) Wannier-Mott exciton in an inorganic lattice, (b) charge transfer (CT) exciton in an organic solid, (c) Poole-Frenkel exciton in an organic solid.

binding energy of the exciton is given by the polarisability of the surrounding material and is used as a measure of distinction between three types of excitons: Poole-Frenkel excitons, charge transfer (CT) excitons and Wannier-Mott excitons (compare figure 1.5). The latter is typically encountered in inorganic materials as it is defined by a binding energy of approximately 10 - 100 meV, which results from screening of the Coulomb attraction by a large polarisability of the surrounding material. As organic materials are characterised by low permittivities ($\varepsilon_r \sim 2-6$), the exciton binding energies are typically much larger, resulting in the formation of CT excitons or Poole-Frenkel excitons (binding energy 0.1 - 1 eV). While a more extensive treatment of excitons is certainly possible, it shall be omitted here as excitonic transport is not important for the understanding of subsequent chapters.

1.2.2. TRAP STATES

An important point to consider when dealing with organic semiconductors is the presence of *trap states*. A trap state is a point at which the local energy is significantly lowered with respect to its surroundings, i.e. more than $k_B T$ beneath the transport level. This low energy site captures passing charge carriers, which are then localised on this site and no longer available for transport unless they can be released thermally (i.e. by phonon scattering). Once trapped, a charge carrier may further hinder charge transport by scattering other free charge carriers through Coulomb interactions.

The origins of traps are manifold: A trap can be created by any kind of impurity in the semiconductor, e.g. ionised dopant molecules (see section 1.3), contaminations in the

material itself (which may partially be avoided by sublimation), remainders of any kind of solvent used during processing or simply degraded semiconductor molecules. Traps are also formed by morphological variations, i.e. at grain boundaries or in the vicinity of material interfaces. In the case of amorphous materials, they can even be caused simply by a high energetic disorder. In the literature, traps are often classified as *shallow* or *deep*, depending on their distance from the respective transport level. Shallow traps typically originate from the static disorder of a material and thus from tail states of the density of states (DOS), while deep traps are more often associated with chemical impurities.

The distribution of traps in a given material can be investigated by various methods, e.g. impedance spectroscopy [25, 26] or the thermally stimulated current (TSC) method [27, 28]. In impedance spectroscopy, the trap distribution is accessed via a small signal AC bias with a varying frequency, where the semiconductor is treated as a capacitive element. The capacitance then changes as a function of frequency, since the time constant for carrier release is inversely proportional to the trap depth. In TSC, traps are first filled either via injection or illumination and subsequently emptied by slowly increasing the sample temperature. The resultant current is measured as a function of temperature and thus yields the trap depth and density. Trap density functions are typically given as either exponential (e.g. as exponential tails to the transport levels) or Gaussian (used more often to describe discrete trap levels) and the total trap distribution in a material may be described as the superposition of several of these functions [29].

As will become apparent in the next paragraph, the investigation of trap distributions in organic semiconductors is of particular importance when attempting to describe charge carrier transport by a theoretical model.

1.2.3. BAND TRANSPORT OR HOPPING TRANSPORT?

The description of charge transport in an organic semiconductor is everything but trivial. Owing to the large variety of molecular structures and film morphologies, a global transport theory would need to be able to bridge the gap between highly ordered materials, which may even be single-crystalline, and increasingly amorphous materials with considerable static energetic disorder. The difficulties which this presents are perhaps best illustrated using the example of charge carrier mobility. In the classical sense, the charge carrier mobility μ is a material-specific parameter which describes the ability of a charge carrier to

move through a material under an external field. In an inorganic semiconductor with weak electron-phonon coupling and thus a standard Bloch electron behaviour, the mobility μ is expressed by the Drude model as

$$\mu = \frac{e\tau(T)}{m^*} \tag{1.4}$$

where e is the elementary charge, $\tau(T)$ is the temperature-dependent mean time between collisions of the charge carrier with an impurity site or phonon and m^* is the effective mass of the carrier originating from band dispersion. For an ideal band transport, the mobility should then present an inverse temperature dependence of the form $\mu \sim T^{-3/2}$ [30] at high temperatures, owing to increasing charge carrier scattering by phonons, while at very low temperatures, the mobility behaves as $\mu \sim T^{3/2}$ due to thermal activation of shallow traps. Ultra-pure organic single crystals do indeed display such a relationship, as shown in figure 1.6 for a perylene crystal. Just like real inorganic semiconductors however, they do depart from the $\mu \sim T^{3/2}$ dependence in the low temperature regime due to broader distributions of shallow traps (rather than the single shallow trap assumed for the ideal scenario) [19]. Such systems of ultra-pure organic single crystals with band-like transport of nearly free charge carriers have shown low-temperature charge carrier mobilities of up to 400 cm^2/Vs [19].

Most organic solids, however, are far from pure and moreover polycrystalline or amorphous, with a considerable static disorder. They consequently show lower mobilities of the order 10^{-5} cm^2/Vs to 1 cm^2/Vs[4] and have a temperature dependence opposite to that of ultra-pure crystals: The mobility increases with increasing temperature. It is believed that the large energetic disorder in these materials results not in the formation of clearly defined energetic bands, but in a broad distribution of molecular HOMOs and LUMOs. As a consequence, it is not possible to describe charge carrier transport by the common band transport model associated with delocalised charge carriers as coherent Bloch waves. Instead, charge carriers are localised on individual molecules and may "hop" to a neighbouring molecule only if the energetic barrier between these molecules can be overcome by thermal activation (see figure 1.7).

Several models have been presented in the literature which deal specifically with either highly crystalline or amorphous materials, i.e. with systems which present either only

[4] More recent efforts to increase charge carrier mobility for polycrystalline systems have resulted in mobilities as high as 43 cm^2/Vs for C_8-BTBT [32], but again the applicability of the processing method to mass manufacturing is questionable.

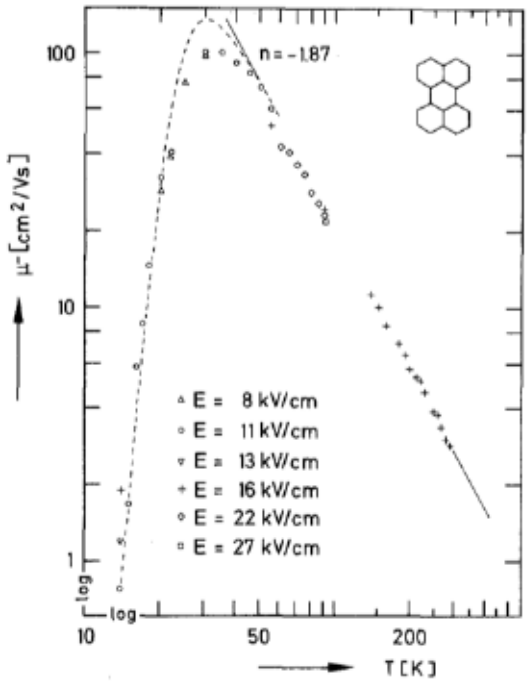

Figure 1.6.: Electron mobility as a function of temperature in perylene in an oblique crystallographic direction [$\measuredangle E,a$ =45(1)°, $\measuredangle E,b$ =66(1)°, $\measuredangle E,c^*$=55(1)°; sample thickness was 370(10)µm]. The broken line is a fit with the Hoesterey-Letson type shallow trapping model [31] with the parameters trap depth, E_{tr} = 17.5 meV, and trap concentration, N_{tr}/N_b = 5 x 10^{-4} mol/mol. Reprinted from ref. [19] with permission of Springer.

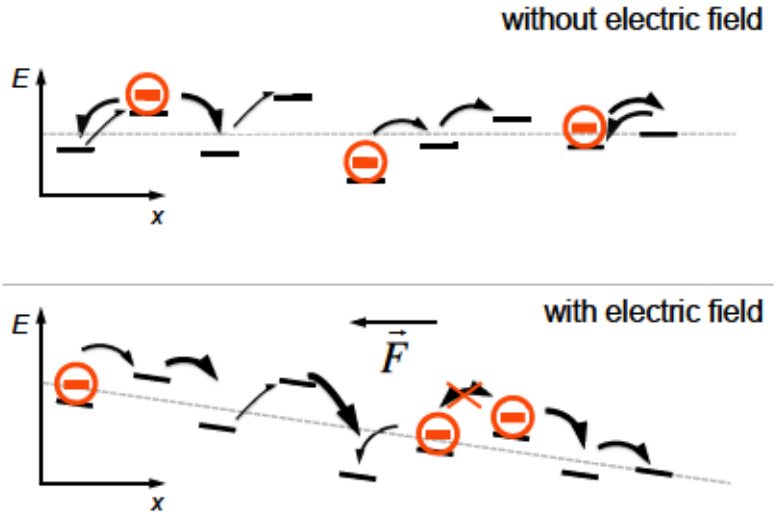

Figure 1.7.: Schematic representation of hopping transport in an energetically disordered organic semiconductor subjected to an external electric field *F*.

dynamic disorder (at high temperatures) or static *and* dynamic disorder. Transport through organic single crystals is often described theoretically by the Holstein model [33, 34] or derivations thereof. This model is derived from the Hamiltonian of an electron-phonon system in organic solids, which, assuming linear interaction, takes the form

$$H = H_{\mathrm{el}}^{0} + H_{\mathrm{ph}}^{0} + \Phi_{\mathrm{el\text{-}ph}}^{\mathrm{local}} + \Phi_{\mathrm{el\text{-}ph}}^{\mathrm{nonlocal}} \tag{1.5}$$

By excluding the nonlocal electron-phonon coupling term, Holstein derived a transport model which explicitly describes a transition from pure band transport at low temperatures to a small-polaron hopping transport at temperatures higher than the Debye temperature of the solid. This results in two separate expressions of the mobility for band-like and hopping transport [22]:

$$\mu_{band} = \frac{ea^2\omega_0}{k_{\mathrm{B}}T}\sqrt{\frac{g^2\mathrm{csch}((\hbar\omega_0)/(2k_{\mathrm{B}}T))}{\pi}}\exp\left(-2g^2\mathrm{csch}\left(\frac{\hbar\omega_0}{2k_{\mathrm{B}}T}\right)\right) \tag{1.6}$$

$$\mu_{hop} = \frac{ea^2J^2}{\hbar^2\omega_0 k_{\mathrm{B}}T}\sqrt{\frac{\pi}{g^2\mathrm{csch}((\hbar\omega_0)/(2k_{\mathrm{B}}T))}}\exp\left(-2g^2\tanh\left(\frac{\hbar\omega_0}{4k_{\mathrm{B}}T}\right)\right) \tag{1.7}$$

Here, ω_0 is the phonon frequency and g, a and J are the electron-phonon coupling constant, the spacing between molecules and the transfer integral. All other variables and constants have their usual meanings. Later works e.g. by Hannewald *et al.* [35], Munn and Silbey [36] and Ortmann *et al.* [37, 38] aim to improve Holsteins model by including also the nonlocal electron-phonon coupling and thus making the model more generally applicable.

Transport through strictly amorphous materials was first described by Miller and Abrahams in 1960. They proposed a mechanism based on phonon-assisted polaron tunnelling [39], which allowed for thermally activated hopping to a nearest neighbour position as well as so-called *variable range hopping* to spatially remote, but energetically favourable states. In this context, the energetic disorder of the system and thus the activation energies for the individual hopping processes are represented by a set of randomly distributed resistors. Based on this principle of simulating an energetically disordered material, Vissenberg and Matters presented a percolation model for the field-effect mobility determined in OFETs based on amorphous materials [40]. They assumed that the high carrier concentration in the active channel region of an OFET would lead to the filling of more localised states and actual traps, so that any excess charge carriers would occupy higher transport

states. Through this mechanism, the activation energy for hops of these excess carriers would be significantly reduced. Consequently, the majority of charge carriers actually contributing to transport in OFETs would, by this theory, be those of the exponential tails in the otherwise Gaussian density of states (DOS). Perhaps the most commonly used hopping transport model today is that of Bässler *et al.* [41], which describes the so-called *diagonal disorder*, i.e. the Gaussian DOS representing static disorder, as

$$G(E) = (2\pi\tilde{\sigma})^{-1/2} \exp\left(\frac{-E^2}{2\tilde{\sigma}^2}\right) \tag{1.8}$$

which has the width $\tilde{\sigma}$. Hopping between two random sites i and j is then described by the hopping rate ν_{ij}, which is constant, if the carrier hops to a site of lower energy, and temperature-dependent (with a Boltzmann term), if the hop occurs across to a site with higher energy:

$$\nu_{ij} = \nu_0 \exp\left(-2\gamma_B a \frac{\Delta R_{ij}}{a}\right) \begin{cases} 1 & \varepsilon_j < \varepsilon_i \\ \exp\left(-\frac{\varepsilon_j - \varepsilon_i}{k_B T}\right); & \varepsilon_j > \varepsilon_i \end{cases} \tag{1.9}$$

Here, ν_0 is a constant pre-factor, γ_B and a are the inverse Bohr radius and the average lattice distance, ΔR_{ij} is the absolute distance between the two hopping sites, k_B and T have their usual meaning and ε_i and ε_j are the energies of the two sites. This model has been developed further by Novikov *et al.* through consideration of the spatial correlation of charge-dipole interactions [42] and by Pasveer *et al.* [43], whose simulation of hopping transport in polymers with a simple uncorrelated Gaussian disorder model (GDM) was able to reproduce experimental results in a wide range of applied fields, temperatures and charge carrier densities.

Horowitz *et al.* suggested a multiple trapping and release (MTR) model, working from the assumption that rather than describing hopping transport by means of Gaussian disorder of the relevant transport states, one should consider a distribution of traps as the limiting factor in real devices [44]. They later modified this model, based on experimental findings, to argue that transport in polycrystalline OFETs can be described by trap-free hopping within individual grains, but is limited by large trap distributions at the grain boundaries, which correlates well with the temperature dependence of the mobility observed in their devices [45].

It is evident from these few examples of transport theories that the transport mechan-

isms themselves are already a matter of much discussion. Which mechanism is dominant in a specific material system or device, however, is an altogether much more complex matter, as this depends not only on the intrinsic properties of the material, but also on its purity and growth conditions. Several measurement techniques, such as optical spectroscopy, Seebeck measurements, electron spin resonance (ESR) or Hall effect measurements can and should be employed to investigate the exact transport mechanisms, since the temperature dependence of e.g. the field-effect mobility, while being a first indicator for either hopping or band transport, does not automatically give a hint to the correct transport model [7].

DEPENDENCE ON CHARGE CARRIER DENSITY AND ELECTRIC FIELD STRENGTH

The Bässler model includes not only a temperature dependence of the mobility, but also a dependence on electric field strength F, since the hopping rate is modified under application of strong electric fields (hopping along the field becomes more probable due to new possible percolation paths, while hopping against the field is less likely to occur). The resultant mobility can thus be expressed a

$$\mu\left(F,T\right)=\mu_0\exp\left[-\left(\frac{2\sigma_E}{3k_BT}\right)^2+C\left(\left(\frac{\sigma_E}{k_BT}\right)^2-\Sigma^2\right)\sqrt{F}\right] \tag{1.10}$$

where σ_E and Σ describe the energetic and spatial disorder of the semiconductor and C is an empirical constant estimated to be 2.9x10-4$\sqrt{\text{cm/V}}$. μ_0 represents the mobility of the material at zero field. A similar expression has also been derived in analogy to the Poole-Frenkel law and is thus called the Poole-Frenkel model [46, 47]:

$$\mu(F,T)=\mu_\infty\exp\left(\frac{\Delta_0-\beta_{PF}\sqrt{F}}{k_BT_{eff}}\right)\ \text{with}\ \frac{1}{T_{eff}}=\frac{1}{T}-\frac{1}{T_0} \tag{1.11}$$

Here, μ_∞, Δ_0, β_{PF} and T_0 are constants. In the case of the Poole-Frenkel mobility, it is assumed that the field dependence originates from a barrier lowering between hopping sites. For small F, the mobility is often observed to become field-independent [43, 48, 49]. A dependence of mobility on charge carrier density has also been reported [41, 50–52], which may be explained using the argument of state occupation: At low charge carrier densities, states with low energy tend to be filled first and it is only at increasing charge carrier densities that higher lying states are occupied. Considering the hopping mechanism,

these higher lying states have a higher hopping rate and thus higher mobility. This effective dependence on charge carrier density has been incorporated by Pasveer *et al.* into the empirical expression

$$\mu(T,F,n) = \mu_0(T)\cdot f(F,T)\cdot g(n,T)$$

$$\text{with } \mu_0(T) = \frac{a^2\nu_0 e}{\sigma_E} c_1 \exp\left(-c_2\left(\frac{\sigma_E}{k_B T}\right)^2\right)$$

$$f(F,T) = \exp\left[0.44\left(\left(\frac{\sigma_E}{k_B T}\right)^{3/2} - 2.2\right)\left(\sqrt{1+0.8\left(\frac{Fea}{\sigma_E}\right)^2} - 1\right)\right]$$

$$g(n,T) = \exp\left[\frac{1}{2}\left(\left(\frac{\sigma_E}{k_B T}\right)^2 - \frac{\sigma_E}{k_B T}\right)\left(2na^3\right)^{\delta}\right]$$

$$\delta = 2\left(\frac{k_B T}{\sigma_E}\right)^2\left[\ln\left(\left(\frac{\sigma_E}{k_B T}\right)^2 - \frac{\sigma_E}{k_B T}\right) - \ln\left(\ln 4\right)\right] \quad (1.12)$$

where c_1 and c_2 are empirical material parameters, a is the effective lattice constant and ν_0 and σ_E are defined in the same way as before [43]. This is also referred to as the Extended Gaussian Disorder Model (EGDM).

It is possible to determine experimentally which of these models applies to a specific material under the given measurement and device conditions. A method for doing so will be presented in chapter 4 of this thesis.

1.3. DOPING OF ORGANIC SEMICONDUCTORS

The term *doping* refers to the intentional addition of impurities into the semiconductor matrix in order to increase electrical conductivity by way of providing additional free charge carriers. This concept has been adopted very successfully in inorganic semiconductors and is now a key component in the manufacturing process of many semiconductor devices, e.g. in MOSFET technology [30]. This same concept may also be applied to organic semiconductors and their related devices. Here, however, rather than having a limited number of atomic dopants to choose from, the variety of suitable materials for either n-type or p-type doping is quite large, since organic semiconductors can be doped by other organic molecules, small atoms and even certain metal complexes. A good general discussion of this topic can be found for example in ref. [7, 20].

The doping process in organic semiconductors is, in essence, similar to that of inorganic semiconductors. Dopant atoms or molecules are chosen such that the LUMO of the dopant is deeper than the HOMO of the matrix (for p-type doping) or the HOMO of the dopant shallower than the LUMO of the matrix (for n-type doping). For the case of p-type doping, this results in the transfer of an electron from the matrix HOMO to the dopant LUMO, which produces an additional hole in the matrix. A p-dopant is therefore also referred to as an *electron acceptor*. In the n-doping process, electrons are transferred from the dopant HOMO into the matrix LUMO so that they are available for charge transport. n-dopants are consequently also called *electron donors*. However, while charge carriers generated by this method in inorganic semiconductors are typically free, the low dielectric constant of most organic semiconductors generally results in the formation of a CT state (as described above), since the charge carrier created in the matrix is still bound by Coulomb interaction to its counterpart on the dopant molecule. Dissociation of this CT state is thermally activated, so that a doping efficiency of less than unity can be expected for many systems at room temperature. The doping efficiency, that is to say the ratio of generated free charge carriers and total number of dopant molecules in the system, is further lowered by the fact that a successful doping process results in the ionisation of the dopant molecule, which may then act as a trap or scattering centre for free charge carriers.

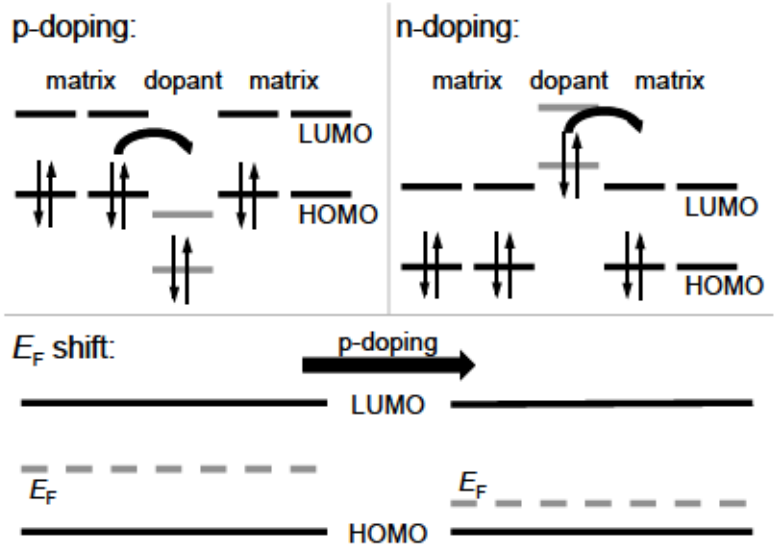

Figure 1.8.: Schematic representation of the p- (top left) and n-doping (top right) process in organic semiconductors and the resultant Fermi level shift (bottom).

If the doping process is successful, i.e. if the density of free charge carriers, n, is increased, this raises the conductivity of the matrix-dopant system, since

$$\sigma = ne\mu \tag{1.13}$$

where σ is the conductivity, e the elementary charge and μ the charge carrier mobility. A rise in n further has the effect of shifting the Fermi level E_F of the matrix towards the respective transport state, as shown in figure 1.8. Experimentally, a rise in n can be investigated e.g. by measuring the change in depletion zone width upon doping in p-i-n or n-i-p diodes, as done e.g. by Olthof *et al.* [53], and its effects on conductivity may be investigated by conductivity measurements on either pure layers of the matrix-dopant system or in an OFET geometry, as will be demonstrated in chapter 7. The energetic distance between the Fermi level and the respective transport state, denoted as ϕ, may be investigated by the Seebeck effect or ultraviolet photoelectron spectroscopy (UPS) [53, 54].

First successful demonstrations of doping in organic semiconductors were provided by Yamamoto *et al.*, who employed strongly oxidising gases as p-dopants [55] and Haddon *et al.*, who used alkali metals for n-type doping [56]. While both approaches demonstrated the desired rise in conductivity, however, the doping effect was found to be unstable, since the small dopant atoms diffused into the matrix. Furthermore, the exact control of the doping ratio proved very difficult for such small atomic dopants. Later efforts to investigate doping in organic semiconductors thus focused on larger molecular dopants and metal complexes. Nowadays, molecular doping is used in OLEDs [57–61] and OPV [62–64] to enhance the bulk conductivity through electron and hole transport layers. It has further been demonstrated to enhance charge carrier injection in OFETs (see section 2.3) and even change a normally n-type material to a p-type material for OFET operation [65]. While these results are conclusive proof that molecular doping of organic semiconductors is possible, the doping process itself is not yet fully understood. For one, the exact molecular arrangement in doped films is unclear for many systems. While atomic dopants in inorganic semiconductors generally sit on the lattice sites, i.e. replace matrix atoms, the large variety of organic dopants and matrix materials alike makes it difficult to come to a general understanding of how dopant and matrix mix, since the behaviour may be different for each system and will greatly influence the electronic properties of the mixed layer.

Clustering of dopants for example, as may happen during evaporation, post-annealing or simply due to ageing, can lead to a decrease of doping efficiency, since only the dopants in direct contact with a matrix molecule can accept / donate electrons. At the same time however, theoretical studies suggest that the interaction of dopant molecules may lead to an increase of doping efficiency due to a lowering of the energy barrier during CT state dissociation [66]. Furthermore, successful p-doping has also been observed for material systems where the dopant LUMO is within the energy gap of the matrix, which - by the above process - should prevent electron transfer to the dopant. It is believed that the doping effect in such scenarios arises instead from a hybridisation of the matrix and dopant energy levels [67, 68], but further studies are certainly necessary to confirm the exact nature of the doping process for each individual system.

2. ORGANIC FIELD-EFFECT TRANSISTORS

In this chapter, one of the most important devices in organic electronics, the organic field-effect transistor (OFET) will be introduced and its functional principles will be explained in detail. Aspects important for OFET operation, such as the interface formation, contact resistance and short-channel behaviour will be discussed and a brief overview of potential applications for OFETs will be given.

So far, the basic properties of organic semiconductor materials have been discussed. The remainder of this chapter will now deal with the use of these materials in actual electronics devices, more specifically in organic transistors.

An organic transistor is a three-terminal device consisting of a gate electrode and dielectric, an active semiconductor layer and a source and drain contact. The general arrangement of these components is adapted from inorganic thin-film transistor (TFT) technology, which is why OFETs are often also termed OTFTs (organic thin-film transistors) in the literature. The different possibilities of arranging the individual components in an OFET can be divided into bottom-gate and top-gate or bottom-contact and top-contact geometries respectively, as illustrated in figure 2.1.

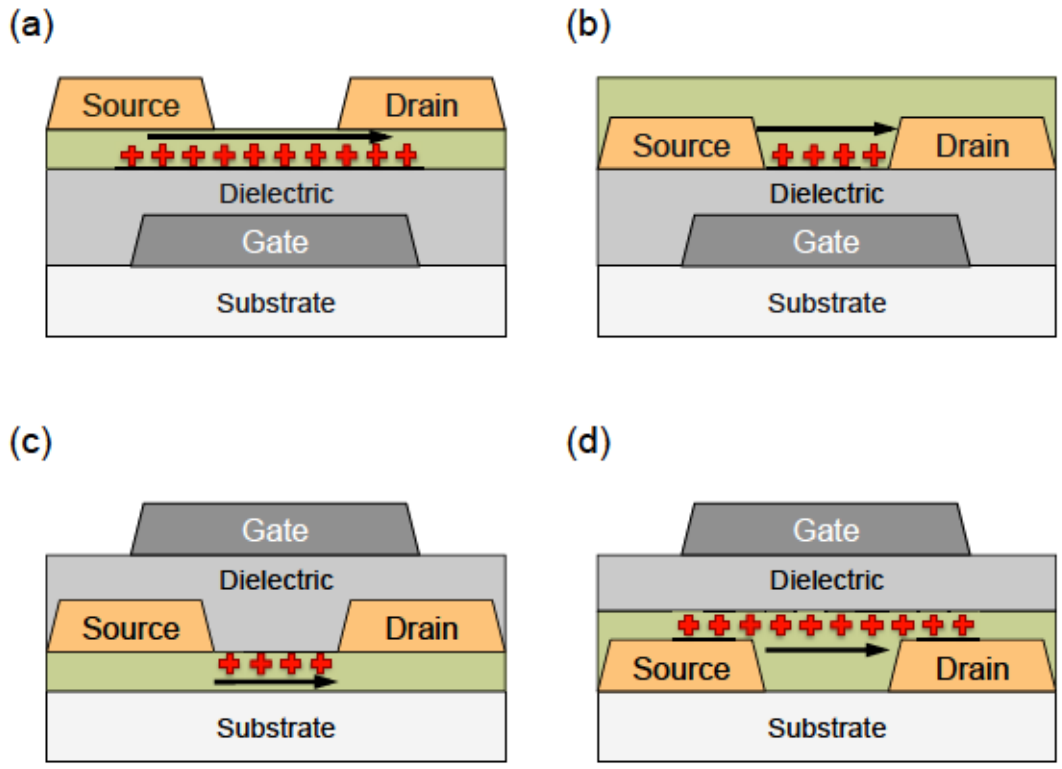

Figure 2.1.: Cross-sectional representations of the different OFET geometries: (a) Bottom-gate, top-contact OFET (also referred to as a bottom-gate staggered OFET); (b) Bottom-gate, bottom-contact OFET (also referred to as bottom-gate, coplanar OFET); (c) Top-gate, top-contact OFET (also referred to as top-gate staggered OFET); (d) Top-gate, bottom-contact OFET (also referred to as top-gate, coplanar OFET).

The first OFETs were realised experimentally as early as the 1980s [69–71] and have since then attracted considerable attention, both as a tool for material characterisation and as a research area in its own right, with a large variety of possible applications. As

with organic LEDs and solar cells, the key features of this technology are its potential for manufacturing on flexible substrates and its low cost due to the very small amounts of materials used in actual devices. Indeed, in terms of organic material usage, the OFET may well be one of the cheapest organic electronic devices, since a single layer of semiconductor, typically less than 100 nm thick, in combination with equally thick metal contacts, as well as an oxide or polymer gate dielectric is sufficient to build a working device. An even simpler setup is the organic metal-semiconductor field-effect transistor (OMESFET) [72, 73], which is different from the conventional OFET only in the sense that it has no gate dielectric and the gate electrode is in direct contact with the active layer. Just like the OFET, this geometry has been adapted from silicon technology, where the MESFET developed as a variation of the standard MOSFET concept. Another derivative of MOSFET technology, the junction field-effect transistor (JFET) has been absent from organic electronics for a considerable amount of time, since the doping technology required to build such a device was not yet established. Only recent advances in the control of the depletion width of an organic pn-junction [74, 75] have lead to the realisation of the organic JFET [76].

2.1. OPERATIONAL PRINCIPLE

As figure 2.1 illustrates, the most common organic transistor, the OFET (or OTFT) can be arranged in different geometries, the only requirement being that the source and drain contacts both have an interface to the organic semiconductor and that the gate electrode is electrically separated from the semiconductor by a suitable gate dielectric. Alternatively, as done for MESFETs, the gate may be separated electrically via a thin depletion layer, which naturally forms when a semiconductor is brought in contact with a metal (see section 2.2). In contrast to MOSFET technology, the organic semiconductor itself is typically undoped, i.e. *intrinsic*. Consequently, most OFETs operate in accumulation mode, i.e. the voltage applied to the gate in the On-state of the transistor is such that majority charge carriers are accumulated at the gate dielectric interface (see figure 2.2) to form a highly conductive channel region through which the majority of the current flows when a voltage is applied also between source and drain. This portion of current constitutes the On-state current of the device and can be controlled by the gate field. The application of an opposite bias

consequently blocks this current path and switches the transistor off. A small portion of charge carriers, however, is always emitted from the source and moves through the bulk of the organic semiconductor. This constitutes the leakage current, also called the Off-state current, as it cannot be blocked by the gate field and is thus present even when the transistor is switched off.

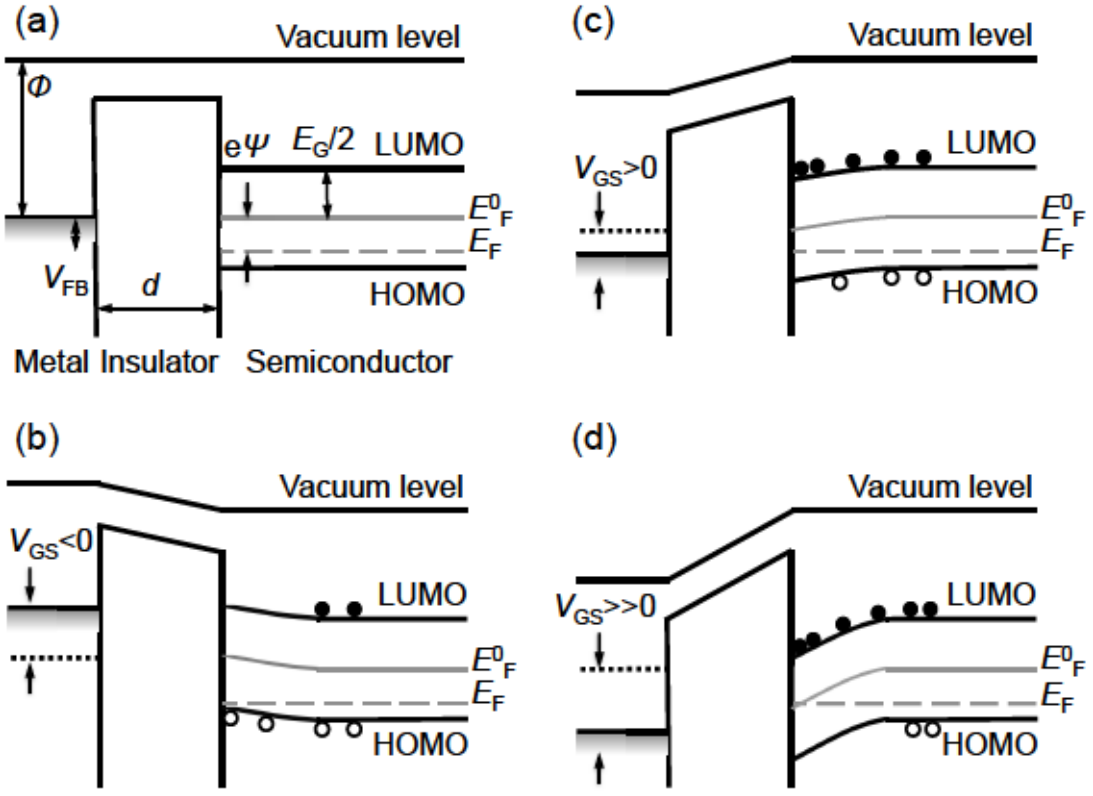

Figure 2.2.: Energy level diagram at the interface between gate, dielectric and a p-type organic semiconductor: (a) No external bias, this is the equilibrium condition of the system. (b) A negative external bias results in hole accumulation at the semiconductor-dielectric interface, this constitutes the On-state of a transistor. (c) A positive external bias causes depletion of holes at the interface, this constitutes the Off-state of a normal OFET or depletion regime of a depletion / inversion OFET. (d) A strong positive bias results in accumulation of electrons, i.e. minority charge carriers, this is the inversion regime. The quasi-Fermi level is denoted as E_F, the Fermi level of the semiconductor in equilibrium is E_F^0 and the workfunction of the metallic gate contact is Φ.

The modulation of the output current I_D (the drain current) by the input voltage V_{GS}, applied between the source and gate contacts, is described by the so-called *transconductance*, g_m:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS}=\text{const.}} \tag{2.1}$$

This transconductance can be extracted from the so-called *transfer curve* of a tran-

sistor, meaning a plot of drain current I_D versus applied gate voltage V_{GS} for a constant source-drain voltage V_{DS}. It is perhaps the most fundamental parameter for characterising the performance of a transistor. Even though the operation mode of an OFET differs from that of a standard MOSFET, it is still possible - to a good approximation at least - to describe the drain current itself by the standard MOSFET formalism [8,30], referred to as the gradual channel approximation. This framework yields two regimes of transistor operation, the linear and the saturation regime. In the linear regime, where $|V_{DS}| < |V_{GS} - V_{th}|$, the charge carrier density is approximately uniform across the entire transistor channel and increases linearly with V_{DS}, consequently the drain current follows the same relationship:

$$I_D = \frac{\mu C_{diel} W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

for $|V_{GS} - V_{th}| > |V_{DS}|$ (linear regime) (2.2)

At the so-called *pinch-off point*, marked by $|V_{DS}| = |V_{GS} - V_{th}|$, a charge depletion zone begins to form at the drain contact due to the reduced drain-gate field. As V_{DS} is increased beyond this point, the charge depletion zone broadens, moving the pinch-off point further towards the source contact. The potential at this point remains fixed at $V_{GS} - V_{th}$, thus the transistor current becomes independent of V_{DS} in this saturation regime:

$$I_D = \frac{\mu C_{diel} W}{2L} (V_{GS} - V_{th})^2$$

for $|V_{DS}| > |V_{GS} - V_{th}| > 0$ (saturation regime) (2.3)

Here, μ is the field-effect mobility of the active semiconductor material, C_{diel} is the capacitance per unit area of the gate dielectric, W and L are the width and length of the conductive channel (given by the width and separation distance of the source and drain contacts) and V_{th} is the *threshold voltage* of the transistor. This latter parameter has been adopted from the MOSFET formalism even though its original definition does not hold for OFETs. In MOSFET devices, V_{th} denotes the minimum gate voltage at which strong inversion may be achieved [30]. Since OFETs operate in accumulation rather than inversion mode, it is obvious that this definition cannot be applied to OFET devices. Nevertheless it is still possible to extract a meaningful value for V_{th} from an OFET transfer curve (as will

be done later in this thesis). This value then denotes the minimum V_{GS} required to obtain 'an appreciable drain current' [8].

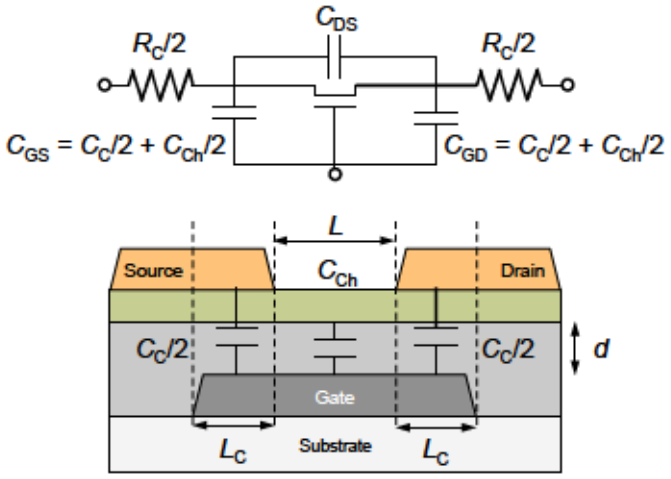

Figure 2.3.: Equivalent circuit diagram of an OFET (top) and schematic representation of a staggered bottom-gate OFET (bottom) with capacitive components indicated as in the circuit diagram.

In order for equ. 2.2 and 2.3 to correctly describe OFET operation, several criteria must be met:

1. The resistance of the conductive channel, R_{Ch} must be significantly larger than the injection / ejection resistance at the source and drain contacts, R_C $\left(R_{Ch} \gg R_C\right)$,
2. the charge carrier mobility, μ, must be constant, i.e. independent of variations in electric field and / or charge carrier density,
3. the distance between the source and drain contacts, i.e. the channel length L, must be much smaller than the width W of each contact $\left(W \gg L\right)$,
4. and the vertical source-gate field must be significantly larger than the lateral source-drain field.

With these assumptions valid, equ. 2.2 and 2.3 can describe the output characteristics of an ideal OFET, as shown in figure 2.4 for a device with a threshold voltage of 0.5 V.

Up to this point it has been assumed that the only current flowing in the OFET is the lateral current between source and drain. For an ideal OFET, this is certainly true, but real OFETs also suffer from a leakage current between the source and gate electrodes[1]. In static conditions, this simply means an additional current component I_G which can be

[1]This is particularly the case for thin gate dielectrics and dielectric materials with large pinholes.

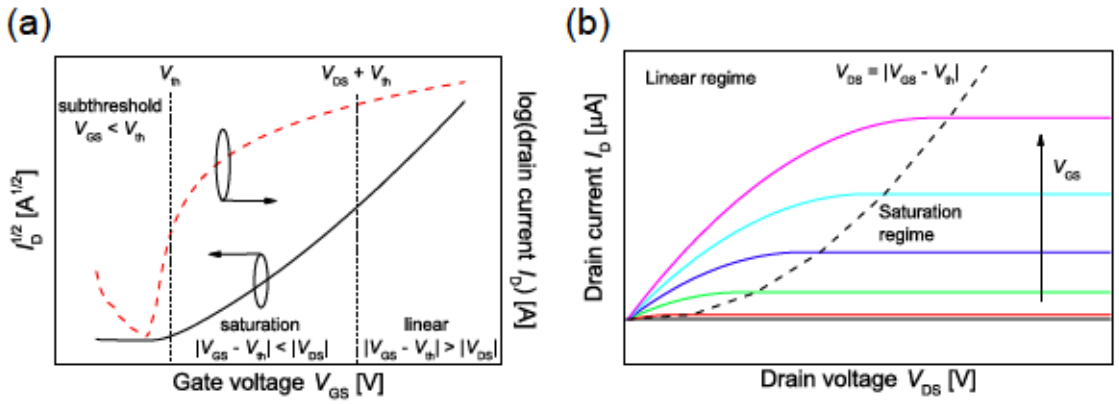

Figure 2.4.: Transfer (a) and output (b) characteristics of an ideal OFET with a threshold voltage V_{th} of 0.5 V. The saturation and linear regimes are marked in both figure parts.

measured between the source and gate and is V_{GS}-dependent. Under dynamic conditions, i.e. when the gate voltage is changed at a frequency f, one must regard the charge flow at the gate as a displacement current of the form

$$i_G = \frac{\partial q_G}{\partial t} = C_G \frac{\partial v_{GS}}{\partial t} = (2\pi f C_G v_{GS})\hat{i} \tag{2.4}$$

where $\hat{i} = \sqrt{-1}$, C_G is the equivalent gate capacitance and i_G and v_{GS} are small signal parameters. From equ. 2.4 it is obvious that the gate current increases with increasing switching frequency. A frequency-dependent current gain of the OFET, i.e. the ratio of drain current to gate current, can thus be defined as

$$\frac{|i_D|}{|i_G|} = \frac{g_m v_{GS}}{2\pi f C_G v_{GS}} = \frac{g_m}{2\pi f C_G} \tag{2.5}$$

It is generally accepted that a transistor whose gate current is higher than the drain current may no longer be operated in a sensible way. This imposes an upper limit on the possible switching frequency of an OFET, the so-called *cutoff frequency*, f_T:

$$f_T = f\left(\frac{|i_D|}{|i_G|} = 1\right) = \frac{g_m}{2\pi C_G} \tag{2.6}$$

The equivalent gate capacitance C_G is given by the combined gate-source and gate-drain capacitances and may be described, using the Miller effect [77], as

$$C_G = C_{GS} + C_{GD}\left(1 + g_m R_{load}\right) \tag{2.7}$$

where R_{load} is the load resistance of the OFET. Equ. 2.7 has a minimum at $g_m R_{load} \sim 0$, and so an upper limit of the cutoff frequency is given by

$$f_T = \frac{g_m}{2\pi C_G} = \frac{g_m}{2\pi \left(C_{GS} + C_{GD}\right)} \sim \frac{g_m}{2\pi CW \left(L + 2L_C\right)} \tag{2.8}$$

where L_C is the source-gate and drain-gate overlap length and all other variables have the same meaning as before. The cutoff frequency can be determined experimentally by a high-frequency characterisation of the OFET. It may also be estimated from the operation of a ring oscillator, as described further in section 2.4.

2.2. FUNCTIONAL INTERFACES IN OFETS

It is evident from the above description of OFET operation that interfaces in the device are of vital importance for the overall charge conduction process, since charge carriers first have to be injected into the OFET via a metal-semiconductor interface and then transported along an insulator-semiconductor interface in order to be extracted again at the other end of the channel. A brief discussion of these two important interfaces thus seems necessary. A more detailed text on this matter may be found e.g. in ref. [24, 78].

2.2.1. DIELECTRIC - SEMICONDUCTOR INTERFACE

The significance of the dielectric-semiconductor interface is clear from figure 2.2: The formation of the conductive channel region and thus charge carrier transport happens in the direct vicinity of this interface. The quality of this interface and the dielectric as a whole is thus of paramount importance for good OFET operation already at low driving voltage V_{GS}. For the interface itself, this means that it should be as trap-free as possible, while the dielectric itself should have a large capacitance per unit area (compare equ. 2.2 and 2.3) $C_{diel} = \varepsilon_r \varepsilon_0 / d$. The latter may be achieved either by a reduction in dielectric layer thickness d or by choice of a material with a high dielectric constant ε_r. A measure of the number of traps at the gate dielectric interface of an OFET is provided by the so-called *subthreshold swing*. This can be extracted from the subthreshold region $\left(V_{GS} < V_{th}\right)$ of the transistor's transfer curve as

$$S = \frac{\partial V_{GS}}{\partial \left(\lg I_D\right)} = \frac{k_B T}{e} \left(1 + \frac{e N_{it}}{C_{diel}}\right) \ln 10 \tag{2.9}$$

where N_{it} is the density of traps at the interface. The term $\left(1 + eN_{it}/C_{diel}\right)$ is also referred to as the ideality factor of the transistor. A FET with no interface traps would have an ideality factor of one, making the ideal subthreshold swing at room temperature equal to 60 mV/decade. Silicon MOSFETs often come close to this value due to the high-quality interface between Si and SiO_2. The interface of organic semiconductors with SiO_2 is usually much less ideal, as is also the case for most other oxide dielectrics, so that the subthreshold swing in OFETs is typically much larger.

While many OFETs use SiO_2 ($\varepsilon_r \sim 3.9$ [79]), e.g. on Si wafers, as the gate dielectric, the subthreshold swing in these devices is indeed considerable, which is attributed to the porous nature of SiO_2. Its surface captures OH-groups which then act as electron traps. Silane-based self-assembling monolayers (SAMs) with hydrophobic end-groups are used in such cases to passivate the oxide surface [80–82]. Several of these SAMs have the added benefit of improving the thin-film growth of polycrystalline small molecule semiconductors, so that the OFET mobility is increased not only due to a decrease of N_{it}, but also due to a more beneficial morphology with less grain boundaries [80, 81, 83]. More recently, it has been demonstrated that even certain small molecules can produce similar effects, when deposited as a thin layer on top of SiO_2 [84–86], and can even facilitate bipolar transport in typical p-type materials [87, 88].

Even with such surface modifications however, SiO_2 is not an ideal material for OFET dielectrics due to the generally large d and small ε of these layers. More recent efforts have therefore concentrated on developing thin oxide gate dielectrics with higher ε, such as e.g. Al_2O_3 ($\varepsilon_r = 4 - 9$ [89–92]), HfO_2 ($\varepsilon_r \sim 16$ [93]), TiO_2 ($\varepsilon_r \sim 21$ [94]), Ta_2O_5 ($\varepsilon_r \sim 21$ [95]) and even aluminium-doped HfO_x ($\varepsilon_r = 11.5$ [93]), which may additionally be patterned to allow for integrated circuit applications. If deposited e.g. via atomic layer deposition (ALD [96]), such high-ε_r dielectrics can form densely packed layers which provide a high breakdown stability even at layer thicknesses below 50 nm and can thus be used to operate OFETs below 10 V. The disadvantage of these materials is that the charge carrier mobility in the OFET drops as the dielectric constant of the insulator is increased. This effect can be observed for polymers and small molecule semiconductors alike and is attributed to charge carrier localisation due to polarisation effects [97–99].

An alternative approach, which circumvents this issue, are polymer dielectrics, e.g. PMMA, PVP or the commercial compound CYTOP. While polymer dielectrics generally have a lower

ε_r (approximately 2 - 4 on average), most of these materials can be easily deposited from solution and are thus interesting for mass manufacturing. Many polymers additionally provide a very low density of interface traps and are thus particularly suited for n-type OFETs, where charge carrier trapping by OH-groups at the gate dielectric interface is an issue. However, OFET operation below $|V_{GS}| = 10\,V$ is rarely observed with polymer dielectrics as their low breakdown fields and the frequent occurrence of pinholes in thin polymer layers make it necessary to keep the dielectric layer thickness well above 50 nm. This problem may be partially overcome by cross-linking or depositing several thin layers of the same polymer [100, 101], yet for very thin gate dielectrics it is still advisable to choose an oxide material.

A very promising method to realise very thin gate dielectrics with acceptable leakage currents is the use of ultra-thin oxide layers in combination with highly insulating SAMs. The group of Hagen Klauk, for instance, has very successfully demonstrated OFETs with operation voltages below 3 V, using a 5.7 nm-thick dielectric made of a SAM and AlO_x, where the thin AlO_x layer is produced by plasma oxidation of the Al gate electrode [102–104].

2.2.2. METAL - SEMICONDUCTOR INTERFACE

When a metal is brought into contact with a semiconductor under equilibrium conditions, i.e. with no external bias applied, the general assumption from classical semiconductor theory is that the vacuum levels of both materials will align, as stated by the Schottky-Mott rule. In the same way, the Fermi level of the semiconductor will align with the metal workfunction. This re-arrangement of energy levels leads to a charge depletion zone at the interface, which can withstand application of an external voltage, yet allows for tunnelling of free charge carriers. In this case, the electron and hole injection barriers from the metal into the semiconductor would simply be given by the energy difference between the semiconductor electron affinity and the metal workfunction / the semiconductor ionisation potential and the metal workfunction. This scenario is displayed in figure 2.5 (a) and is often assumed to be valid also for organic semiconductors [78].

However, UPS studies on several metal-semiconductor interfaces have shown that the Schottky-Mott rule does not necessarily hold for real interfaces [24]. Instead, an

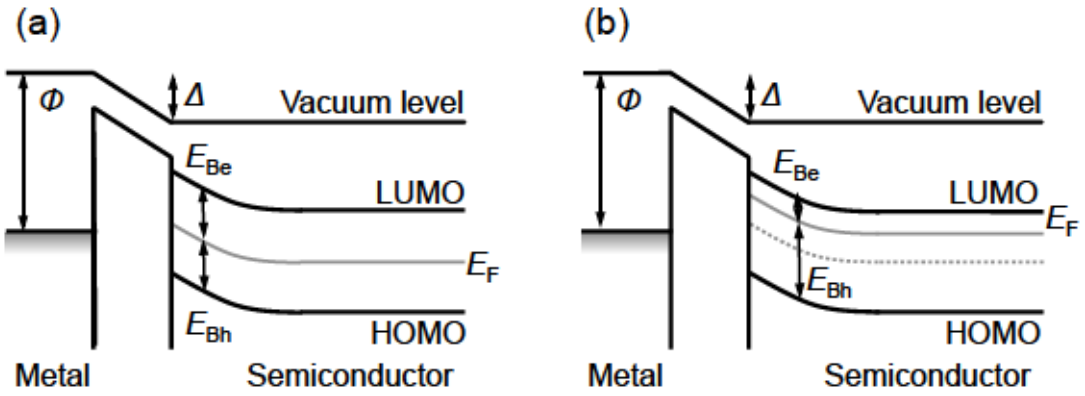

Figure 2.5.: Energy level diagrams for a metal-semiconductor interface according to the Schottky-Mott rule (a) and with an interface dipole, as predicted by the Bardeen limit (b).

injection barrier more similar to the Bardeen limit[2] has been found e.g. for pentacene on gold [105, 106]. While Bardeen attributed the origins of such a dipole to a large density of surface states caused by the dangling bonds in inorganic semiconductors, the absence of precisely these dangling bonds at the surface of organic semiconductors (due to the strong localisation of charge carriers) requires a different explanation for the dipole formation. Possible reasons for the dipole formation in this case may be a chemical reaction at the interface, a charge transfer between the metal and the semiconductor (the *image-force effect*, also present in inorganic semiconductors), an orientation of permanent dipoles in the organic semiconductor or the so-called *pillow effect*, i.e. a compression of the tail states of the metal DOS [24, 107, 108].

CHARGE CARRIER INJECTION UNDER BIAS

When an additional bias is applied (in the case of an OFET, this is V_{GS}), the resultant electric field F affects also the metal-semiconductor interface so as to enhance charge carrier injection. This is illustrated in figure 2.6 (a). The electric field provided by the applied gate voltage V_{GS} shifts the energy levels of the organic semiconductor so that they form a linear gradient (dashed line in figure 2.6 (a)). As e.g. an electron is injected into the semiconductor at a distance x from the interface, a positive image charge is formed in the metal, at the same distance from the interface. This image charge creates a so-called

[2] In this limit, the energy barrier height becomes independent of the metal workfunction and is instead given by $E_b = E_G - E_F^0$, where E_F^0 is the semiconductor's Fermi level pinned by surface states.

image potential

$$\Phi_{\text{image}} = \frac{e^2}{16\pi\varepsilon_r\varepsilon_0}\frac{1}{x} \tag{2.10}$$

The superposition of this image potential (grey line in figure 2.6 (a)) and the potential created by V_{GS} reduces the injection barrier height by

$$\Delta\Phi = \sqrt{\frac{e^3 F}{4\pi\varepsilon_r\varepsilon_0}} \tag{2.11}$$

The maximum of this barrier is located at a distance x_m from the interface, given by

$$x_m = \sqrt{\frac{e}{16\pi\varepsilon_r\varepsilon_0 F}} \tag{2.12}$$

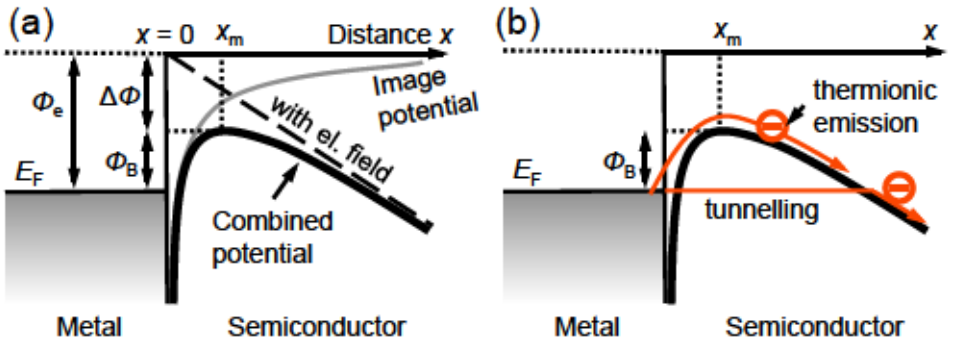

Figure 2.6.: Injection barrier lowering by the Schottky effect under application of an external electric field F: Φ_e and $\Phi_B = \Phi_e - \Delta\Phi$ are the injection barrier heights without and with image charge lowering. x_m denotes the width of the injection barrier. Interface dipoles due to effects other than image charges have been excluded in this picture for simplicity.

Charge carriers may be injected across this lowered barrier by two different mechanisms (see figure 2.6 (b)): A charge carrier may either have sufficient energy to overcome the barrier, which is referred to as *thermionic emission*, or it may tunnel through the barrier via the field-effect (also referred to as *Fowler-Nordheim tunnelling*). For real Schottky barriers, carrier injection for charge carriers with an energy between E_F and $E_F + \Phi_B$ is best described by the term *thermionic field emission*, as the two mechanisms presented above are really limiting cases [9]. The total current across the real Schottky barrier can be estimated for the case $eV > 3k_BT$ as

$$I = \frac{4\pi e m^* (k_B T)^2}{h^3} \exp\left(-\frac{\Phi_B}{k_B T}\right) \exp\left[\left(\frac{eV}{\gamma k_B T}\right) - 1\right] \tag{2.13}$$

where V is the voltage drop across the barrier and γ is an ideality factor ($\gamma = 1$ for ideal Schottky diodes) [9].

From this discussion it is evident that the height of the injection barrier at the OFET's source / drain contacts is another important criterion for OFET operation. Since the semiconductor itself is intrinsic, especially an efficient injection is essential for good performance. This will be dealt with in more detail in the next section, where the general effects of contact resistance on a device are discussed.

2.3. CONTACT RESISTANCE AND SHORT-CHANNEL EFFECTS IN OFETS

The gradual channel approximation relies on the assumption that the channel resistance is the dominant resistance in an OFET, i.e. that resistance at the contacts (due to energy barriers) is negligible in comparison. The channel resistance is naturally determined by the length L of the channel. L, in turn, is given by the distance between the source and the drain contact and so the minimum of L achievable in a real OFET depends on the resolution of the structuring method used to structure the source and drain contacts on the substrate / dielectric (for bottom-contact configurations) or organic semiconductor (for top-contact configurations). Since many applications of OFETs require high switching frequencies and On-state currents, it is often desirable to reduce L as much as possible. Equally, materials with higher and higher charge carrier mobilities are continuously being developed (compare figure 2.9). The overall effect is the continuous decrease of channel resistance in real OFETs, which necessarily makes contact resistance an increasingly important factor for transistor performance. Furthermore, the aggressive downscaling of transistor channel length leads to the occurrence of so-called short-channel effects. Since both effects will be important for the vertical transistor geometry investigated in this thesis, they shall be discussed in more detail in the following paragraphs.

2.3.1. CONTACT RESISTANCE

The term contact resistance actually refers very broadly to any resistance that is not strictly associated with the conductive channel, but is located within the direct vicinity of the injection / ejection area. Consequently, it can be separated into two major contributions:

- actual injection / ejection resistance due to the Schottky barrier at the metal-semiconductor interface (see section 2.2)

- resistance of the bulk semiconductor underneath the contacts, which limits the access to the conductive channel and is also referred to as *access resistance*

While the latter is of course absent in coplanar devices (see figure 2.1 (b) and (c)), it must be considered for staggered geometries and may there contribute significantly to the overall contact resistance. An important factor to consider in this context is the thickness of the active semiconductor. To reduce access resistance, it is generally beneficial to keep the semiconductor layer as thin as possible [109, 110], yet lower limits to the thickness are often imposed for polycrystalline materials due to the need to form a closed semiconductor layer in the channel region. Furthermore, as several groups have shown, the deposition of the metal contacts on top of an organic semiconductor can lead to metal diffusion (for low metal deposition rates), dislodging of organic molecules and even thermal damage to the organic film (at high deposition rates) [109, 111–113]. As Sawabe *et al.* have argued, the diffusion of Au into Pentacene, while generally disturbing the energetic order of the film, can also be beneficial, since it provides a series of gap states above the Pentacene HOMO through which charge carrier conduction may take place [111]. This, in the authors' view, may actually reduce the contact resistance, rather than increasing it.

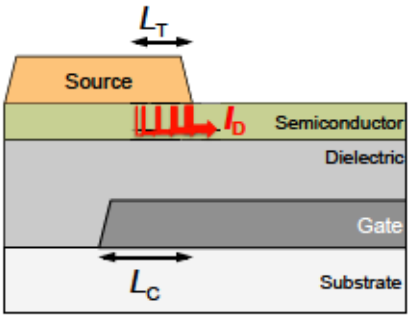

Figure 2.7.: Schematic representation of the injection area underneath the source contact of an OFET with current flow as proposed by the crowded current model.

The general effect of the access resistance is described within the crowded current model (see figure 2.7) [114, 115]. Here, an effective injection / ejection area of the contacts is defined, which is small if the specific channel resistance per unit area, r_{Ch} is large compared to the specific contact resistance per unit area, r_C, but takes the dimensions

$A = WL_T$ when $r_{Ch} < r_C$. L_T is the so-called *transfer length* of the OFET and is given by

$$L_T = \frac{R_C W}{r_{Ch} \coth\left(L_C/L_T\right)} \approx \frac{R_C W}{r_{Ch}} \text{ for } L_C \gg L_T \tag{2.14}$$

where L_C is the gate-source overlap. For the case $L_C < L_T$, as may occur for structured gate electrodes, the OFET would indeed be injection-limited. Both the contact resistance and transfer length can be accessed experimentally via the transmission line method (TLM), which will be explained in detail in section 4.3.2. Measurements of contact resistance using this technique, as well as results from four-point measurements, have shown a dependence of contact resistance and transfer length on V_{GS} [110, 116]. This is considered within the crowded current model: An increased gate voltage leads to a lowering of the channel resistance, thus broadening the effective emission area (i.e. increasing L_T). Furthermore, the conductivity of the bulk semiconductor underneath the contacts is increased due to a higher charge carrier density, which is provided by gate-induced charges [115].

In real OFET devices, a weak contact limitation $\left(R_C < R_{Ch}\right)$ is often observed and manifests itself as a decreased saturation current as well as a weaker increase of current in the linear regime (in comparison to the ideal device), as demonstrated in figure 2.8. A strong contact limitation $\left(R_C > R_{Ch}\right)$ leads to a non-linear behaviour of the drain current for small V_{DS}. This is typically only observed if the Schottky barrier at the contact is particularly high (due to a bad choice of material) or the transistor channel is particularly short. This second limiting case must indeed be considered separately, as it brings about several other effects as well.

The high-frequency switching of OFETs is also affected by contact resistance. Hoppe *et al.* have therefore derived an expression for the cutoff frequency f_T in the linear regime, which accounts not only for the overlap capacitance, but also for contact resistance [117]:

$$f_T = \frac{\mu V_{DS}}{2\pi L^2} \cdot \frac{L^2}{\left(L + L_T\right)^2} \cdot \frac{L}{L + L_C} \tag{2.15}$$

The first term of this expression represents the cutoff frequency obtained for an ideal OFET without contact resistance or parasitic electrode overlap. The second term modifies this ideal cutoff frequency for the occurrence of noticeable contact resistance and the third term accounts for the parasitic contact overlap. The resultant cutoff frequency in a

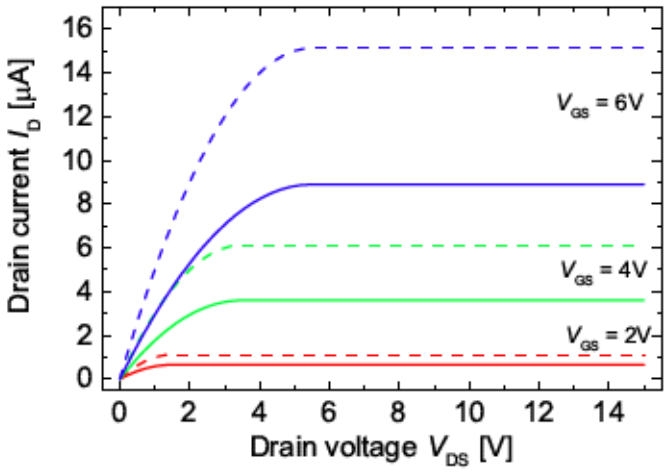

Figure 2.8.: Output characteristics of an ideal OFET (dashed lines) and a real OFET with weak contact limitation (solid lines).

non-ideal transistor is thus significantly lowered by both effects.

Contact limitations in OFETs can be overcome by careful engineering of the contacts[3]. This includes the correct choice of electrode material and deposition parameters as well as the concept of contact doping. Here, the electrode-semiconductor interface is selectively doped by inserting a thin layer of either pure dopant or a matrix-dopant system in order to improve injection into the channel region. This has successfully been demonstrated by many groups [102, 119–123]. In particular, Ante *et al.* have shown the reduction of contact resistance for a thin layer of pure dopant and also demonstrated a reduction in required transfer length for the doped devices. This result is of considerable interest, as it allows for reduction of the source-gate overlap and general downscaling of the electrode dimensions, so as to provide a smaller parasitic overlap between source and gate [102]. The concept of contact doping, as well as its exact effects on transistor performance and the origins for improvement, will be discussed in more detail in chapter 7.

2.3.2. SHORT-CHANNEL BEHAVIOUR

The so-called *short-channel behaviour* arises when the channel length in OFETs is scaled down so aggressively that the last assumption stated previously for the gradual channel approximation no longer holds, i.e. when the source-drain distance becomes so short that the source-drain field is comparable to the source-gate field. In addition to contact limitation, this naturally leads to deviations from the ideal OFET output characteristics

[3]A comprehensive review on contact engineering has recently been published by Liu *et al.* [118].

predicted by the gradual channel approximation:

- Saturation is lost due to the channel length modulation effect and may be replaced by a space-charge-limited current regime (SCLC)[4],
- a threshold voltage roll-off is observed,
- the subthreshold region of I_D as well as the mobility μ become V_{DS}-dependent.

All these effects have been observed in experiment [124–130], yet channel length modulation is perhaps the most noticeable of these effects. It arises from the fact that the pinch-off point, marking the beginning of the depletion zone near the drain electrode, moves further into the channel as V_{DS} is increased, thus reducing the effective channel length. While this effect always takes place, a loss of saturation only occurs when the size of the depletion region becomes comparable to the effective channel length. The drain current then takes a for which, according to Locci *et al.*, is more suitable described by an SCLC regime forming inside the extended depletion zone [130]. If this SCLC regime is weak (i.e. if the depletion region behaves almost like an ohmic resistance), a good approximation of the drain current at $|V_{DS}| > |V_{GS} - V_{th}| > 0$ may also be given by a simple linear relationship:

$$I_D = I_D^{\text{saturation}} \left(1 + \lambda V_{DS}\right) \tag{2.16}$$

where λ is a fit parameter which is inversely proportional to L. The threshold voltage roll-off and the V_{DS}-dependence of the subthreshold region, as well as the mobility, can be explained by the increased significance of the source-drain field. As stated in section 2.1, the source-drain field causes a certain amount of charge carrier injection into the semiconductor bulk, which is considered as leakage current. In short-channel devices, due to the considerably higher source-drain field, this leakage current may in fact represent a major contribution to the total current of the OFET. In limiting cases, this may even result in a change of OFET operation from normally Off-state to normally On-state, so that the gate voltage is now required to deplete the transistor channel. It is therefore this additional charge carrier injection which causes the observed threshold voltage shift as well as the

[4]The SCLC regime describes a scenario where injection from a contact into an organic semiconductor is more efficient than the drift transport through that semiconductor, so that charges pile up near the injecting contact. Characteristic of such a regime is a quadratic voltage dependence of the current density, with a further dependence on semiconductor layer thickness, scaling with L^{-3}. This will be discussed further in chapter 4.

V_{DS}-dependent subthreshold current. Under these strong fields, as argued by Locci *et al.*, a Poole-Frenkel-type channel mobility of the form $\mu \sim \sqrt{F}$ (see section 1.2) may also have to be considered.

As argued already by standard textbooks for the case of short-channel silicon MOSFETs, it is possible to prevent the occurrence of these short-channel effects if one scales not only L, but also the channel width W and the thickness of the dielectric layer, d, accordingly. Long-channel behaviour should thus be observed even for short-channel devices, provided that the gate-source field is higher than the source-drain field by a factor ≥ 10 [30].

2.4. APPLICATIONS OF OFETS AND RELATED DEVICES

The basic OFET geometry discussed so far can already be used for several different applications, such as radio-frequency identification tags (RFID), control matrices for active-matrix OLED displays (AMOLED displays), etc. The geometry may also be modified in order to realise new functional devices. In this section, a few examples for applications of OFETs shall be given in oder to highlight the versatility of these basic electronics components.

2.4.1. DETERMINATION OF MOBILITY

As has already been stated, OFETs are often used for material characterisation, more specifically for the determination of the charge carrier mobility in newly developed organic semiconductors. Equ. 2.2 and 2.3 can be re-arranged to yield the field-effect mobility of the organic semiconductor layer in the linear and saturation regime

$$\mu_{lin} = \frac{L}{C_{diel} W V_{DS}} \frac{\partial I_D}{\partial V_{GS}} \tag{2.17}$$

$$\mu_{sat} = \frac{2L}{C_{diel} W} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2 \tag{2.18}$$

Indeed, the more thorough understanding of the OFET's functional principles developed in recent years, together with the continuously growing variety of organic semiconductors and sophisticated preparation techniques have lead to the realisation of many high-mobility devices [18, 32, 131]. Yet, as argued by Hagen Klauk in his review on OFETs [8], the field-effect mobility measured in ambient conditions seems to have stagnated in recent years despite the continuous development of new materials. One reason for this may be

that research has not yet produced the one perfect material which is air-stable and yields high mobilities even without the use of complex processing techniques. Another reason is certainly to be sought in the measurement setup itself, i.e. in the OFET geometry.

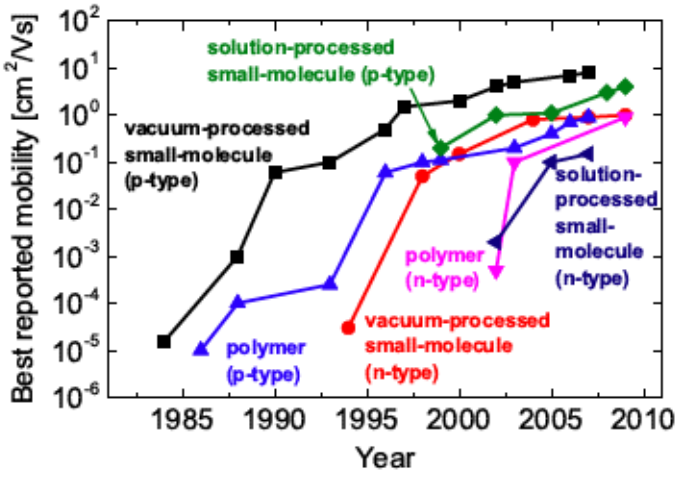

Figure 2.9.: Evolution of the field-effect mobility measured for organic semiconductors in ambient conditions, adapted from ref. [8] with permission from The Royal Society of Chemistry.

The mobility determined from equ. 2.17 and 2.18 is only ever an effective mobility, i.e. it is influenced by such effects as contact resistance or traps at the gate dielectric interface. A reliable value of the mobility may thus only be extracted from long-channel OFETs ($L > 100\,\mu m$, in this case it may be assumed that $R_{Ch} \gg R_C$) with well-designed interfaces. A further problem is presented by the choice of regime from which to extract the mobility. While Horowitz argued that the linear regime should be used for mobility determination due to the varying potential (and thus varying mobility) along the channel in the saturation regime [24], it is common practice to quote precisely this average mobility in the saturation regime, the argument being that the current measured in the saturation regime is limited by the channel, whereas the linear current regime is more likely to be contact-limited. In any case, the mobility values determined from OFET measurements should be treated with care, as they may be valid only in a specific device geometry and under certain measurement conditions.

2.4.2. LOGIC CIRCUITS

Organic transistors can also be combined into more complex integrated circuitry, as required e.g. for RFID tags. The most basic logic components in this context are inverters

and ring oscillators. The inverter is supposed to switch the voltage level of an input signal, i.e. a 'low' V_{in} results in a 'high' V_{out} and vice versa. This may be achieved by connecting two transistors together, as shown in figure 2.10. These may either be of the same type (n- or p-type) or of different types (n- and p-type). The former is referred to as a unipolar inverter, while the latter is called a complementary inverter. Complementary inverters are commonly used in MOSFET technology, since their gain (the maximum of the curve $|dV_{out}/dV_{in}|$, occurring at a voltage V_M, where both FETs have the same conductance) is generally higher than that of a unipolar inverter. The challenge for organic complementary inverters is to find n- and p-type semiconductors whose general properties and OFET behaviour complement each other so as to make the inverter as efficient as possible. This is not always easy, especially if the inverter is required to work under ambient conditions, where n-type semiconductors are often inferior to p-type materials. Furthermore, it must be possible to fabricate the two OFETs in very close vicinity to each other, which can be of particular difficulty when using solution-processed materials. Unipolar OFETs on the other hand, while easier to realise experimentally, have the inherent drawback of inferior performance, since the second OFET, used as a load resistance, prevents the inverter from reaching the two possible extremes (0 V and the supply voltage V_{DD}). As a consequence, unipolar inverters generally present a potential difference between the supply node and the output node, which leads to static current flow and thus higher power consumption compared to the complementary inverter.

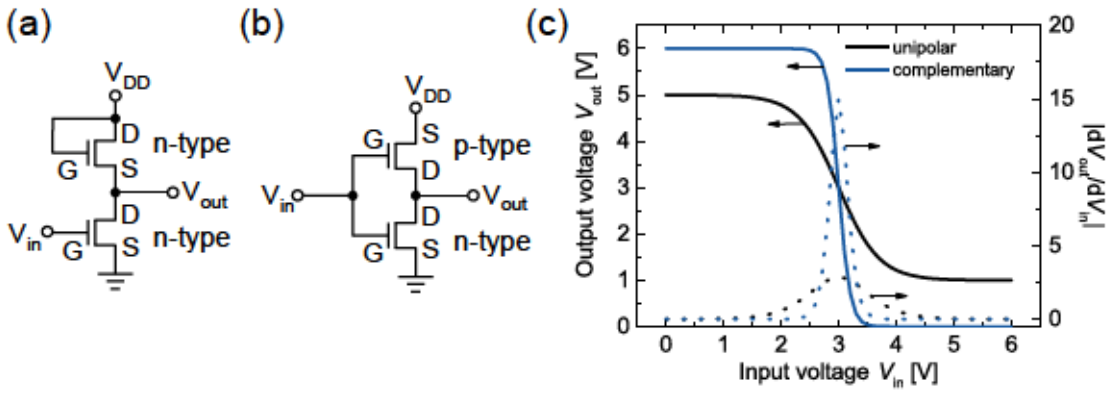

Figure 2.10.: Circuit diagrams of (a) a unipolar inverter with a load transistor and (b) a complementary inverter. The respective output vs. input curves are shown in (c).

Nevertheless, both complementary and unipolar organic inverters have been realised experimentally[5]: Huang *et al.* recently demonstrated a unipolar pentacene inverter where the required threshold voltage control was achieved by UV/ozone treatment of the polymer dielectric [133]. Through this method, they were able to achieve a gain of 14 and a noise margin $\geq$ 70%. Meanwhile, Hunter *et al.* have demonstrated a simple spray-coating technique to fabricate p-type unipolar inverters in a way more suitable to mass production [134]. While the gain of these inverters is only on the order of 6.5, they can be operated well below 10 V. Complementary inverters have also been realised and the issue of finding suitable material pairs has been solved in many different ways. Several groups have combined p-type organic semiconductors with n-type oxide semiconductors to circumvent the problem of finding suitable n-type organic materials [135–137], while others have managed to find suitable combinations of organic materials [138–140]. In a somewhat different approach, Khim *et al.* used molecular doping in order to enhance the ambipolar properties of PCBM and thus realise a complementary inverter based on a single semiconductor [141]. In all these cases, gains well above 10 were achieved, together with noise margins beyond 50%.

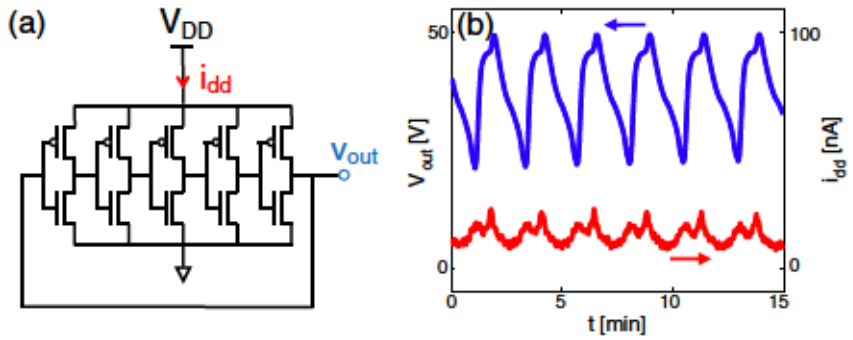

Figure 2.11.: Circuit diagram (a) and output characteristics (b) of a 5-stage complementary ring oscillator, reprinted from ref. [142] with permission from Elsevier.

A ring oscillator is simply a series connection of an odd number of inverters, as illustrated in figure 2.11 (a). The output of the last inverter is fed back into the input of the first inverter. An input signal switch from 'low' to 'high' at the first inverter will cause its output to switch from 'high' to 'low'. This signal change propagates through each inverter (stage) of the ring oscillator and in each inverter there is a certain time delay between receiving the input signal and switching the output signal (due to the capacitive elements in the

[5]A recent review by Mandal and Noh summarises the advances in printed circuits [132].

inverters). This is referred to as the *stage delay*. When the last inverter in the ring oscillator has switched its output, this is fed back to the first inverter as the input signal, thus flipping the first inverter again. The overall effect is that the output of the ring oscillator switches between 'low' and 'high' at a period equal to twice the number of inverters multiplied by the stage delay. If one denotes this period as τ_{osc}, it is possible to estimate the cutoff frequency f_T of a single OFET from a unipolar ring oscillator containing such OFETs, since

$$\tau_{osc} = n_{inv}\tau_{inv} \sim \frac{n_{inv}}{2f_T} \tag{2.19}$$

where τ_{inv} is the stage delay of a single unipolar inverter (containing two OFETs of the same kind) within the ring oscillator and n_{inv} is the number of inverters within the oscillator.

Many 5-stage ring oscillators have been reported in the literature, both unipolar and complementary. Cai *et al.* recently reported a unipolar ring oscillator based on solution-processed single crystals [143]. While such devices certainly have the potential for high performance, the oscillator in this paper operated with a frequency of only 512 Hz, which was attributed to a large contribution of contact resistance in the OFETs. In contrast, Kitamura *et al.* developed a complementary ring oscillator with Pentacene and C_{60} OFETs which operates at frequencies up to 200 kHz [144]. More complex organic circuits, such as NAND gates or full RFID tags have also been realised [136, 145].

2.4.3. MEMORY DEVICES

A more recent development in the field of OFET applications is the organic transistor memory. Memory devices, in particular non-volatile memory devices[6], are required for many applications, such as RFID tags. Particularly in simple, low-cost and low-power-consumption applications it is strictly necessary that these devices be non-volatile, as power to refresh them on a regular basis may not be available. Such non-volatile memory components can be realised with OFETs, where the conventional dielectric is replaced by a ferroelectric material. The resultant hysteresis effect in the OFET may be used to store information. Here, the writing process occurs by application of a gate voltage, which polarises the gate dielectric and thus alters the charge carrier density in and conductivity of the OFET channel. Read-out is done by application of a small drain voltage (to pre-

[6] Inorganic memory devices are often based on capacitors, which tend to leak and thus need to be 'refreshed' every so often. These are termed volatile memory devices.

vent accidental switching of the polarisation). This concept has been adopted by many groups [146–148] and has been used to realise a random access memory (RAM) cell [149]. A current challenge of ferroelectric OFET memories lies in the fact that the ferroelectric layer seems to depolarise in the Off-state of the device. This effect could be counteracted if the semiconductor could supply compensatory charges [148]. Alternatively, one may use different approaches to creating the electrical hysteresis necessary for memory operation. Among the suggested pathways to achieve this are nanoparticles as a chargeable layer at the gate dielectric interface [150], non-polar polymer dielectrics [151], SAM dielectrics [152] and floating gates [153].

Another issue faced in the ferroelectric approach is the driving voltage of the memory device. To reduce power consumption in real applications, this voltage should be small, but this necessitates thin gate dielectrics. As pointed out by Naber *et al.*, a thin ferroelectric layer at the gate may be depolarised by band bending of the semiconductor near the interface, as this induces a potential [148]. While it is of course possible to investigate the band bending of a given material system and use only those semiconductors whose band bending does not depolarise the ferroelectric layer, the required driving voltage can also be reduced by using ambipolar rather than unipolar devices. In this case, however, the ratio of programmed to erased signal is decreased in comparison to unipolar devices. Recently, Lee *et al.* have proposed what they call a 'quasi-unipolar device', where an n-type fullerene layer is embedded into a p-type Pentacene layer. The resultant memory device is believed to harvest electrons from the n-type layer for programming and erasing, thus reducing the required drive voltage, while the reading process occurs through the p-type channel of the underlying pentacene, thus maintaining the high ratio of programmed to erased signal [151].

2.4.4. SENSORS

The electronic properties of many organic semiconductors are sensitive to a whole variety of influences, among them illumination, contact with certain gasses and even mechanical deformations. While for integrated circuit applications, this means that organic electronic devices have to be protected from these influences (e.g. by encapsulation), the same property may deliberately be used to operate the OFET as a sensor: The OFET is driven at a constant V_{GS} and V_{DS} (usually in the saturation regime, as this provides the most stable

behaviour) and the change in output current due to illumination, pressure, gas exposure etc. is measured.

It is immediately obvious from the development of organic solar cells that certain organic materials are very light-sensitive and generate a considerable amount of charge carriers upon illumination. This fact is utilised in organic photo-transistors [154], where the requirement on the semiconductor is that it must not only be highly photo-active, but also have a high charge carrier mobility, so that charges generated in the channel under illumination reach the drain electrode of the OFET and thus contribute to the On-state current. The figures of merit for such devices are the photoresponsivity, R, and the photosensitivity, P, given by

$$R = \frac{I_{light} - I_{dark}}{I} \text{ and} \tag{2.20}$$

$$P = \frac{I_{light} - I_{dark}}{I_{dark}} \tag{2.21}$$

where I_{light} and I_{dark} are the OFET On-state currents with and without illumination and I is the intensity of the incident light. Single crystal silicon photo-transistors may reach values of $R = 300\,AW^{-1}$. Single crystal organic photo-transistors have been shown to exceed this value by far, Kim *et al.* for example demonstrated an anthracene single crystal photo-transistor with $R = 10^4\,AW^{-1}$ and $P = 1.5x10^5$ [155]. Photo-transistors based on polycrystalline thin-films exhibit slightly lower performance due to the lower charge carrier mobility, yet they too are capable of outperforming silicon photo-transistors with highest reported values of $R = 2500 - 4300\,AW^{-1}$ and $P = 4x10^4$ [156]. The general advantage of the photo-transistor over competing technologies, such as diode-based photodetectors, is the low noise level facilitated by the photocurrent amplification.

In OFET-based gas sensors, the change in On-state current required for sensing is generally facilitated by a chemical reaction between the semiconductor surface and the analyte. This reaction may result in a charge transfer between the analyte and the semiconductor, thus changing the charge carrier density in the channel, or it may result in a change of charge carrier mobility or electronic properties of the semiconductor. Since chemical reactions tend to have longer time constants than photo-generation of charge carriers, the response time of OFET gas sensors is much longer than the response time of photo-transistors (by approximately an order of magnitude). The strength of the signal further depends on the interaction strength between the analyte and the

semiconductor, so that careful material design may be required to get the optimum response for specific analytes. This response may be further enhanced by micro-structuring the organic semiconductor to provide a larger reaction interface, as demonstrated for Pentacene OFETs with a rubbed surface [157], where the altered morphology of the pentacene due to rubbing allowed for better diffusion of the analyte (in this case NO_2) into the channel region. Typically, this kind of sensor is only sensitive to a limited number of analytes, depending on which analytes react well with the chosen semiconductor material. However, in a recent study on both n-type and p-type gas sensors, Zang *et al.* have shown that OFET sensors which originally do not show any sensitivity to a particular analyte, may be forced to react with this analyte if previously exposed to a different gas, which itself provides a reaction interface for the analyte [158]. This discovery, if applicable to more semiconductor materials, may provide a simple means to increase the number of analytes which may be detected by a single material OFET sensor.

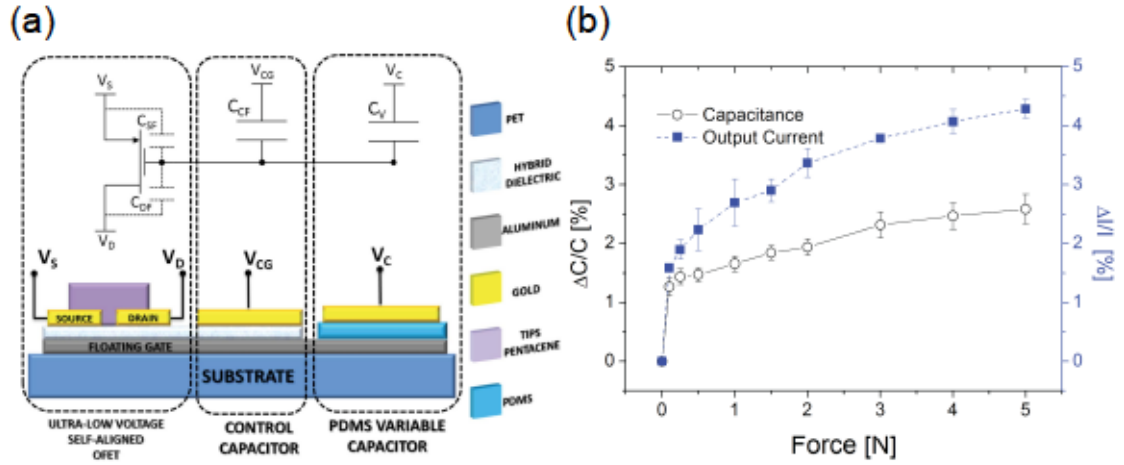

Figure 2.12.: OFET-based pressure sensor by Lai *et al.*: (a) Device setup and material summary and (b) comparison of the variation in OFET output current and PDMS capacitance with applied force. Reprinted from ref. [159] with permission from IEEE.

As a last example of organic sensing devices, OFET-based pressure and mechanical sensors will briefly be discussed. Again, there are many different routes to realising such a device and it is far beyond the scope of this thesis to describe them all. Exemplary here are perhaps the works of Annalisa Bonfiglio's group, as they demonstrate two very simple and elegant approaches to realise such sensors. Cosseddu *et al.* showed that basic Pentacene OFETs on flexible substrates can act as strain sensors if the Pentacene grains in the channel region are large. In this case, the mechanical deformation of the substrate

will lead to significant variation in the distance between individual grains, which in turn affects the OFET output current [160]. Similarly, they concluded that in order to reduce the mechanical sensitivity of polycrystalline OFETs for other applications, it is advisable to deposit the semiconductor under conditions where it forms very small crystallites, as such a film is much less sensitive do bending of the substrate. Lai *et al.* modified a coplanar bottom-gate OFET in order to realise a highly-sensitive pressure sensor. The setup of this device is shown in figure 2.12 (a). Its operational principle is based on the fact that a pressure applied to the PDMS variable capacitor will compress the PDMS layer, thus changing its capacitance and therefore the charge distribution in the floating gate. This change can be monitored directly, making a simple capacitive element sufficient for pressure sensing. The incorporation of the OFET, however, provides an amplification of the signal and thus a much higher sensitivity (see figure 2.12 (b)).

The further development of all these sensor devices, as well as their combination and integration into advanced circuitry, opens up entirely new applications, particularly in the field of bio-sensing and medical sciences, where they might, for instance, serve as components for fully functional, fully flexible and self-powering artificial skin [161].

2.4.5. DISPLAY BACKPLANES AND LIGHT-EMITTING DEVICES

Another important application for OFETs is the driving of OLEDs in AMOLED displays. Such displays, while already commercially available, currently possess control matrices made from amorphous silicon (e.g. Samsung) or oxide semiconductors (e.g. LG) and are thus not fully flexible. As demonstrated recently by the companies Novaled and Plastic Logic (Dresden, Germany), the replacement of these rigid matrices by an OFET control matrix facilitates the full flexibility for which OLED display producers ultimately aim [162].

The simplest way to construct such a driving matrix is illustrated in figure 2.13: The pixels are addressed row-by-row, so that the first step in switching a pixel on or off is to apply a high voltage signal to the respective row. This switches the selection transistor T1 to the On-state. In order to turn the pixel on / off, a high / low voltage is then applied to the respective column. By this signal, the total pixel capacitance, consisting of C_S and the gate dielectric capacitance C_2 of the driving transistor T2, is charged and thus acts as a continuous signal supply when the transistor T1 is switched off again (this is done by providing a low voltage to the row once all pixels in the row have been programmed). If

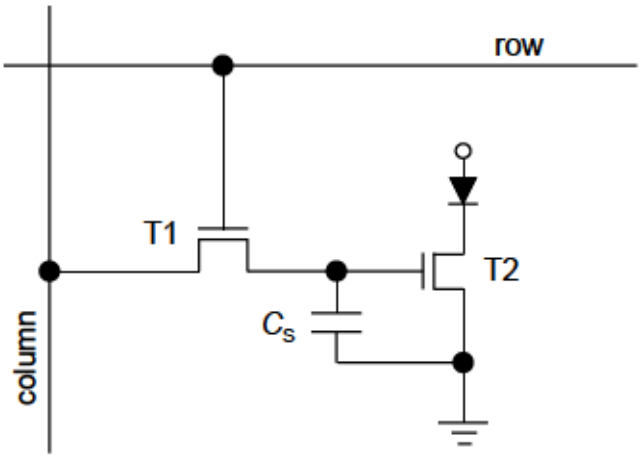

Figure 2.13.: Example of a driving circuit for an OLED in an AMOLED display using n-type transistors. The circuit consists of a selection transistor (T1), a driving transistor (T2) and a storage capacitor C_S.

the voltage applied to the column is high, it switches on T2 and thus the OLED is switched on (and vice versa). This operation mechanism imposes several requirements on T1 and T2, which have been discussed by Gu and Forrest in 1998 [163]. Following this line of thought and using typical parameters for an average display today[7], one finds that the minimum requirements for T1 are a mobility $\mu_1 \frac{W_1}{L_1} \geq 1.2\,\mathrm{cm^2/Vs}$ and an On/Off ratio $\geq 10^6$. Similarly, the requirements for T2 are $\mu_2 \frac{W_2}{L_2} \geq 0.4\,\mathrm{cm^2/Vs}$ and an On/Off ratio $\geq 10^4$, as well as a high threshold voltage stability[8]. While many of the OFETs published to date meet these requirements on a lab scale [164, 165], the challenge for display manufacturing is to fabricate OFETs of the same quality on a large scale and with the stability required for market applications.

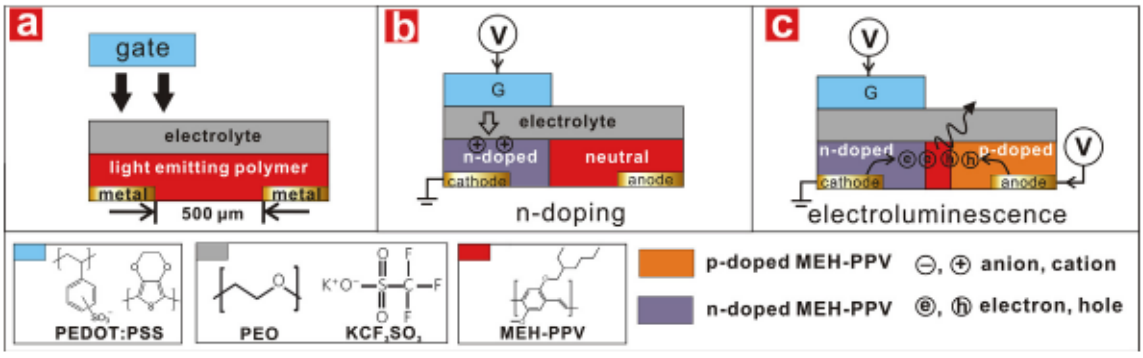

Figure 2.14.: Example of a light-emitting OFET structure, reprinted from ref. [166] with permission from Elsevier.

[7] Display resolution of 326 dpi, frame rate of 120 fps, aperture ratio of 90 %, driving voltages of 3 V, capacitance of T2 of 800 nF/cm^2.

[8] Although instabilities can be compensated by suitable circuitry, this requires additional components and thus makes the backplane more complex and expensive.

More recently, several groups have concentrated their efforts on simplifying the construct of AMOLD displays by combining the switching properties of the OFET and light emission of the OLED into a single device, a light-emitting OFET [154]. This may be achieved e.g. by replacing the conventional semiconductor inside the OFET by a single light-emitting material reducing the dimensions of the gate electrode, so as to artificially form a p-i-n-like structure in the emission layer [166] (see figure 2.14). An alternative method is the vertical stacking of transport and emission layers, as demonstrated e.g. by Maasoumi *et al.* [167], or a combination of horizontal and vertical structuring of the required organic layers [168]. Unfortunately, many of these devices currently lack the brightness, efficiency or stability required e.g. for display applications, however they are powerful tools to study charge carrier flow and recombination and further research in this area may yet produce a device suitable for advanced market applications.

3. VERTICAL ORGANIC TRANSISTORS

This chapter introduces a new device class, the vertical organic transistor. The different device concepts belonging to this class will be looked at in more detail and similarities and differences between these devices and the conventional OFET will be highlighted. The last section in particular will focus on the vertical organic field-effect transistor, its proposed working mechanism and the many questions still to be answered regarding this device.

One might gather from the previous section that OFETs are very versatile devices and are already used in a wide range of applications. This assumption, however, is only partly true. OFETs are indeed very versatile devices and scientific literature provides ample examples for their applications, yet the total market revenue of organic electronics to date is dominated by OLEDs, in particular OLED displays for mobile phones and flat-panel TV screens. One reasons for this may be the lack of high-mobility n-type materials, which are needed for high-performance complementary circuits. Furthermore, while excellent performance of p-type (and sometimes even n-type) OFETs is frequently reported in the literature, many of these results are difficult to reproduce on a mass manufacturing scale, i.e. with simple processing techniques. Another general problem of OFETs is the observed decrease of drain current over time as a constant bias is applied (referred to as *bias stress*, see ref. [169] for a comprehensive discussion of this effect). While it is generally believed that the bias stress is caused by ion migration, charge carrier trapping and perhaps even breaking of molecular bonds within the semiconductor, further research into the origins of bias stress is necessary in order to fully understand and then compensate this effect efficiently to achieve devices with a good performance stability. Next to stability, another requirement for mass market applications, particularly for AMOLED displays, is a high integration density of devices. The aggressive downscaling of OFET dimensions necessary to fulfil this criterion may be achieved quite easily in coplanar bottom-gate or staggered top-gate devices (see figure 2.1 (b) and (c)), since the critical dimensions (the contact size and separation) can be scaled down using standard high-resolution structuring methods. For staggered bottom-gate or coplanar top-gate devices (figure 2.1 (a) and (d)) this is not possible, as the contacts have to be structured on top of an organic layer and many structuring techniques are damaging to organic materials (due to high energy processes or solvent involvement).

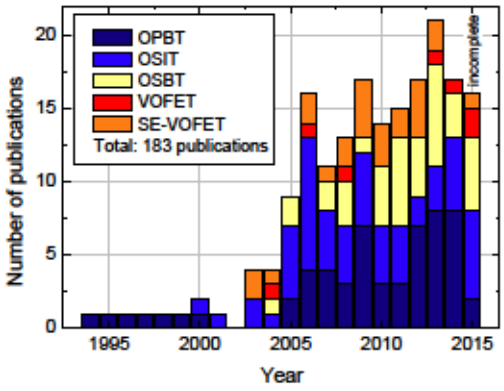

Figure 3.1.: Publications per year for the different architectures of vertical organic transistors: Organic permeable-base transistors (OPBTs), organic static induction transistors (OSITs), organic Schottky barrier transistors (OSBTs), vertical organic field-effect transistors (VOFETs) and their sub-category of step-edge VOFETs (SE-VOFETs). Reprinted from ref. [170] with permission from IOP Publishing.

Vertical organic transistors present a simple approach to reducing lateral device dimension without the need for high-resolution structuring techniques. Vertical organic transistors can be loosely sorted into four categories [170]: organic Schottky barrier transistors (OSBTs), organic permeable-base transistors (OPBTs), organic static induction transistors (OSITs) and vertical organic field-effect transistors (VOFETs). These will all be discussed separately in the following sections as their operational principles are all slightly different. The common denominator between these different geometries is the fact that they are all three-terminal devices (like the OFET) operating in a transistor-like fashion. Unlike the OFET, however, the injecting and ejecting contacts are not arranged in parallel to each other, but are stacked vertically on top of one another. Depending on the geometry, the third contact, which controls the current between the former two, may either be placed above/underneath the injecting and ejecting contacts or it may be placed in-between these two contacts. The great advantage of this vertical stacking approach lies in the significant reduction in substrate area required to build a working device. Furthermore, it is quite simple to stack additional electronic components on top or underneath such a vertical transistor. This results in an instantaneous increase in integration density. As an added benefit, the channel length of such vertical devices is no longer limited by any structuring method (as is the case for the distance between the source and drain contacts of OFETs), but by the layer thickness of the organic semiconductor(s) between the contacts. As will be seen in the following sections, this enables channel lengths of 100 nm or less.

3.1. ORGANIC PERMEABLE-BASE TRANSISTORS (OPBTS) AND ORGANIC STATIC INDUCTION TRANSISTORS (OSITS)

3.1.1. OPBTS

The setup and operational principle of organic permeable-base transistors is similar to that of the vacuum triode and was first presented by Yang and Heeger in 1994 for a polymer OPBT [171]. The OPBT consists of three contacts, stacked vertically on top of each other, with two layers of organic semiconductor in-between (see figure 3.2). The top and bottom electrode are used as the injection and extraction contact, typically referred to as *emitter* and *collector*. The electrode in the centre of the device is referred to as the *base* and is used to manipulate the current flow between emitter and collector. For this purpose, it must be transparent for charge carriers, so that they may pass through it on their way from the emitter to the collector. The current injected into the device at the emitter under forward bias of the emitter-base diode is denoted as I_E. This current is only partially transmitted through the base in a real device, since a non-ideal base electrode will collect some of that current, denoted as I_{EB}. The transmitted portion I_{EC} is drained at the collector if the base-collector diode is operated in reverse. This also results in some current injected from the base into the base-collector diode, so that the total current at the collector is $I_C = I_{EC} + I_{BC}$. The switching between the On- and Off-state of the OPBT is done by controlling the potential difference V_{BE} between the emitter and base, as this controls the amount of current injected into the device, while V_{EC} merely supports an efficient transport through the device.

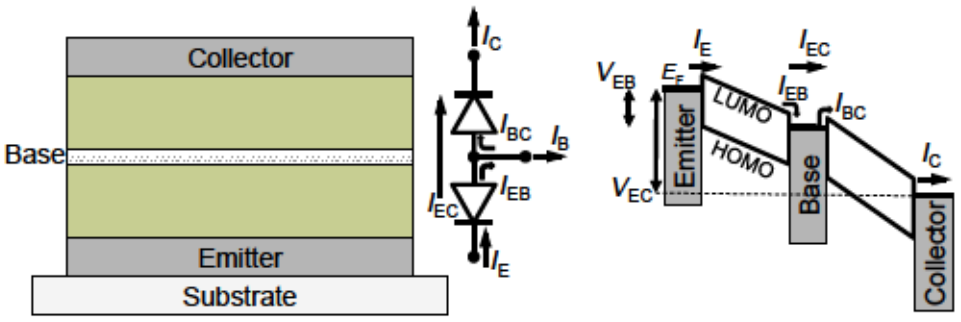

Figure 3.2.: Schematic representation of an organic permeable-base transistor with equivalent circuit diagram and energy level diagram.

In order to quantify OPBT performance, two parameters are of importance: The transmission coefficient α, which describes the ratio of transmitted current to total injected current, and the current amplification β, which describes the ratio of transmitted current to the current lost at the base. These two factors can be expressed as

$$\alpha = \frac{I_{EC}}{I_E} = \frac{I_C - I_{BC}}{I_E} \tag{3.1}$$

$$\beta = \frac{I_{EC}}{I_{EB}} = \frac{I_C - I_{BC}}{I_B - I_{BC}} = \frac{\alpha}{1-\alpha} \tag{3.2}$$

From these two equations it is obvious that a good OPBT should have a large I_{EC}, as this results in a high transmission coefficient (approaching unity) and a high current amplification. The base electrode is thus the key component within the OPBT and the focus of most OPBT research, as it needs to be highly transparent for charge carriers injected at the emitter, yet be insulated well enough in order to reduce leakage currents into the base.

Base electrodes in OPBTs are typically very thin metal films, nanowire networks or carbon nanotube (CNT) networks as these layers provide the best transmission properties. Charge carriers may pass such layers via two methods: In the case of thin, but closed metal layers, a so-called hot carrier transmission process takes place [172–174]. This process is illustrated in figure 3.2 for an n-type OPBT. Due to the potential difference between the emitter and base, a charge carrier injected into the base has an energy somewhat higher than the Fermi level of the base. Under normal circumstances, the carrier will be scattered several times within the base electrode and thus relax to the Fermi level. This can be quantified by the mean free path λ_B. However, if the base electrode is very thin and its injection barrier at the emitter side is higher than that at the collector side, there is an increased probability of the carrier reaching the collector side of the base without being scattered. Such carriers are referred to as hot and are able to overcome the Schottky barrier at the collector side of the base.

As the efficiency of this process very much depends on the electrode material and preparation conditions, the transmission factors determined fur such hot carrier OPBTs are often rather low. Values of $\alpha = 0.1$ and $\alpha = 0.7$ have been reported for aluminium base electrodes [174, 175]. Cheng *et al.* improved the hot carrier process by introducing a series

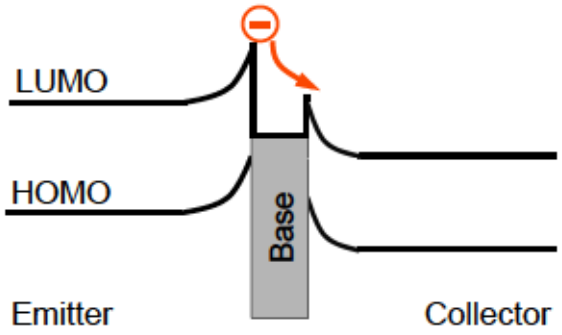

Figure 3.3.: Schematic representation of the hot carrier transmission process through the base electrode of an OPBT: A charge carrier is emitted into the base from the higher lying transport level of the organic semiconductor. If the base is thin, there is an increased probability of the carrier not being scattered within the base so that it still has sufficient energy to overcome the injection barrier at the other end.

of organic semiconductors between the emitter and base of a p-type OPBT, each with a slightly deeper HOMO than the previous layer. Through this ladder-like approach, they were able to increase the energy of the hot carriers considerably and thus reach transmission coefficients up to $\alpha = 0.99$ [176]. While such transmission coefficients are highly desirable, the great advantage of OPBTs - their simple structure - is reduced significantly if such ladder architectures should prove necessary in order to reach these performance values. Furthermore, the careful design of energy barriers at the base electrode may be realised on the lab scale, but it is to be expected that the reproducibility in mass manufacturing is considerably lower.

It has been argued that high transmission rates in OPBTs are not due to efficient hot carrier transport, but due to microscopic perforations of the base electrode through which carriers may pass directly into the base-collector diode [171, 177, 178]. Such pores or pinholes may randomly form in sufficiently thin metal films due to the interaction energies of the metal and the underlying surface (in this case the organic semiconductor of one of the diodes) [177]. Pinhole formation can also be provoked e.g. in aluminium base electrodes by co-evaporation with an organic semiconductor [179] or a metal which can easily be oxidised by thermal annealing in ambient conditions [180]. As Fischer *et al.* have shown for the OPBT structure originally proposed by Fujimoto *et al.* [181], the formation of these pinholes leads to a bidirectional operation of the OPBT, which would not be possible based on a hot carrier mechanism [182].

Operation of the OPBT via pinhole formation in the base electrode provides another

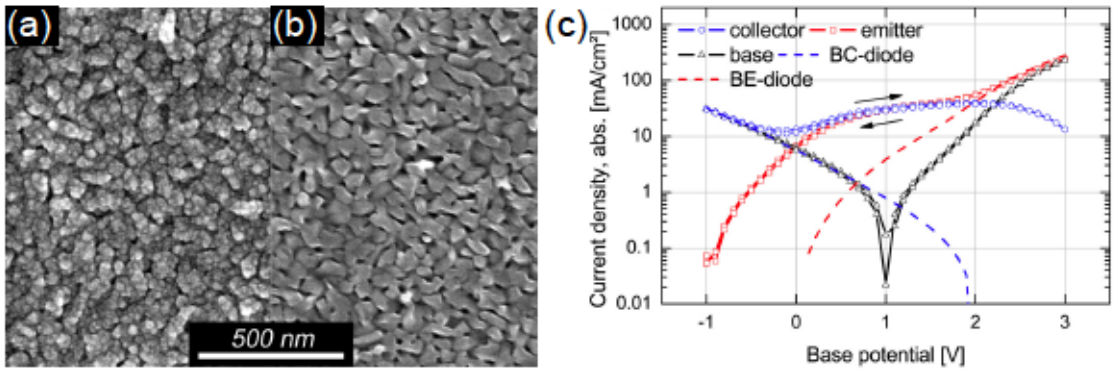

Figure 3.4.: (a) SEM image of the 20 nm Al base electrode used by Fischer *et al.* on 100 nm Me-PTCDI and 50 nm Al. (b) SEM image of 100 nm Me-PTCDI on 50 nm Al for comparison. The roughness features of the Me-PTCDI film observed in (b) are almost exactly mirrored in the base electrode in (a). A base sweep of an OPBT containing such a base electrode is shown in (c) with the top electrode as the emitter and a common-emitter connection with V_{EC} = 2 V. Reprinted from ref. [177] with the permission of AIP Publishing.

advantage over the hot carrier approach: The base electrode, if consisting e.g. of Al, may be oxidised by exposure to air, so that a thin layer of AlO_x insulates the base electrode and thus reduces leakage currents [177, 182, 183]. A recent theoretical study by Chen *et al.* predicts that such devices, if improved further with respects to On-state current, could be an excellent candidate for low-cost, easily fabricated organic electronic devices operating in the GHz regime [184].

3.1.2. OSITS

Strictly speaking, organic static induction transistors are a particular kind of permeable-base transistor. The key difference between these devices and the OPBTs discussed before is the use of common structuring techniques to actively pattern the base electrode. This may be done e.g. by placing a monolayer of polystyrene spheres onto a bottom contact and evaporating a suitable insulator and base electrode material on top of this layer. Subsequent removal of the spheres leads to a base electrode grid with circular openings whose size can be controlled by the size of the polystyrene spheres (see figure 3.5). As this structuring method is both simple and quick, it is used by many groups working in the field of OSITs [185, 186], but structuring via laser holography [187], UV interference lithography [188], nano-imprint lithography [189], shadow mask [190] and e-beam lithography [191] have also been reported.

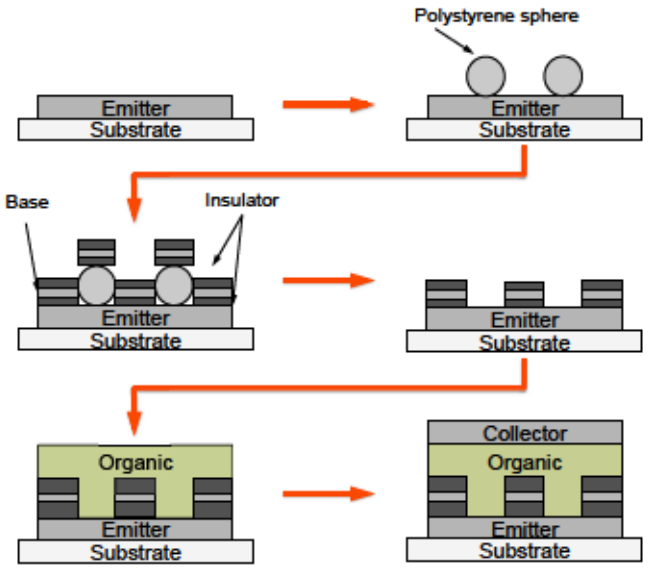

Figure 3.5.: Schematic of the patterning process of an OSIT using polystyrene spheres.

While the pinholes in normal OPBTs are generally small (see figure 3.4), the openings in the base of OSITs are typically 100 - 200 nm in diameter [185] or even larger [190], depending on the structuring technique used in individual cases. This can lead to a somewhat different device behaviour: If the pinholes in OPBTs are small, the base electrode may still shield the collector field, so that the current injected from the emitter is independent of the potential difference between emitter and collector (as is the case for hot carrier OPBTs). The larger opening in OSIT base electrodes provide no such shielding. Furthermore, the openings are expected to be large enough so that they do not represent a bottleneck for charge transport. OSIT devices are therefore largely expected to operate on the principle of space-charge limited currents [185, 189].

Still, treatment of the base electrode and particularly insulation of the base electrode's surface is a key feature to realise high On/Off ratios [188, 192]. Trap formation near the base electrode or the insulators surrounding it may be prevented by treatment with a suitable SAM. This reduces bias stress effects, as shown e.g. by Lin *et al.* [186].

3.2. ORGANIC SCHOTTKY BARRIER TRANSISTORS (OSBTS)

Organic Schottky barrier transistors are perhaps the simplest of the vertical organic transistor architectures. In a broad sense, they may be described as simple organic Schottky diodes which are controlled by a gate contact underneath. One might thus refer to them

also as *switchable organic diodes*. In order for the gate electrode to have any effect on the OSBT, the source electrode must be permeable for DC fields, which is again achieved by using perforated electrodes. The Schottky barrier then limits the Off-state current of the OSBT, while the gate field lowers this barrier in the On-state and thus increases charge carrier injection into the diode. This concept was first introduced by Ma and Yang in 2004 [193] and has since then been adopted by many groups due to the simplicity and versatility of the structure. Using this concept, memory devices [194] and light-emitting transistors [195, 196] have been realised.

3.2.1. SOURCE PERFORATION

The first reported OSBT relied on a source electrode similar to the base electrode in OPBTs: By depositing only a thin metal bi-layer of Cu and Al onto a supercapacitor cell, Ma and Yang ensured a surface roughness of this electrode sufficient to form pinholes, which were then filled by the organic semiconductor C_{60} [193]. They later replaced this metal bi-layer by a single Al layer of ≤ 20 nm thickness [195, 197, 198] and demonstrated via UPS measurements that the gate electrode could indeed modulate the injection barrier between the Al source electrode and the semiconductor above [199]. The screening effect of the source, still present due to the small perforation size, was compensated by the high gate capacitance of the supercapacitor [193]. Particularly their first work demonstrated excellent performance, with an On/Off ratio > 10^6 at a current density in the On-state of 4 A/cm^{2}and an applied gate bias of only 5 V.

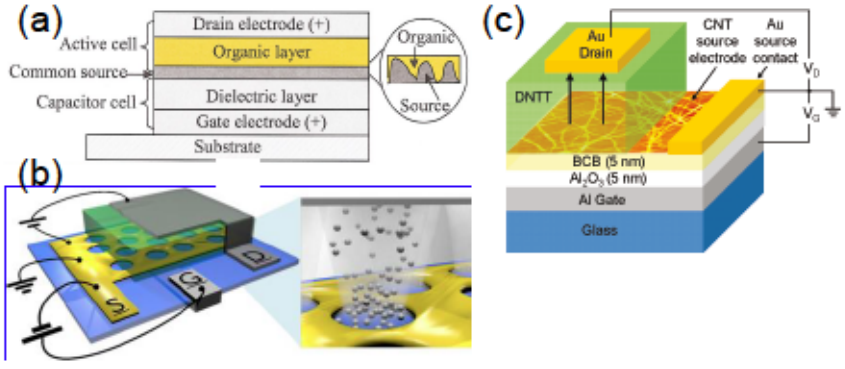

Figure 3.6.: Schematic representations of the different source electrode architectures used in OSBTs: (a) The porous source of Ma and Yang, (b) the patterned source of Ben-Sasson *et al.* and (c) the carbon nanotube (CNT) electrode introduced by McCarthy *et al.* Reprinted from ref. [193, 200, 201] with the permission of AIP Publishing and the American Chemical Society.

In 2009, Ben-Sasson *et al.* modified the approach of Ma and Yang to include an actively patterned source electrode [202]. They used a block co-polymer (BCP) template to realise a 10 nm Au source electrode with cylindrical openings of approximately 80 nm diameter, arguing that a larger perforation size than that used by Ma and Yang would decrease the screening effect of the source and thus reduce the need for high gate capacitance [202, 203]. While these devices show similar current densities in the On-state, the On/Off ratio of the patterned source OSBTs is generally lower [202, 204]. As replacement of the patterned source by a grid of metallic nanowires did not improve upon this fact [205], it is to be assumed that the excellent On/Off ratio of Ma's device was indeed facilitated by the supercapacitor rather than the injection barrier between the source and semiconductor [1]. Nevertheless, later work of Greenman *et al.* was able to demonstrate very high current densities of 3 A/cm^2 and switching within 1 - 2 µs [206].

The flexibility of the OSBT concept was demonstrated by Liu *et al.* in 2008, who not only replaced the porous source electrode of Ma and Yang by a network of single wall carbon nanotubes (CNTs), but also inserted an OLED stack in place of the single semiconductor used until then [207]. The resultant device was termed a Vertical Organic Light-Emitting Transistor (VOLET) and was later optimised to include emission layers for red, blue and green light, selectable by different bias conditions of the gate [196]. Lemaitre *et al.* further improved the original OSBT design by replacing the CNT source electrode by a perforated graphene sheet [208], which improved the On/Off ratio of p-type OSBTs beyond 10^6 for On-state current densities of 200 mA/cm^2.

3.2.2. OPERATIONAL PRINCIPLE

As Xu *et al.* have shown by their UPS studies, the OSBT does indeed rely on manipulation of the Schottky barrier between the source contact and the organic semiconductor. For the case of Ma's device, this manipulation is facilitated by a so-called supercapacitor cell, which produces a high gate dielectric capacitance in ambient conditions due to the formation of mobile ions inside the dielectric. Li *et al.* have shown by temperature-dependent measurements of the output characteristics that if the motion of these ions is slowed down by low temperatures, the transistor performance drops considerably [198]. This

[1] In fact, the device of Ma and Yang must be assumed to have a relatively low Schottky barrier as the workfunction of Cu is approximately 4.7 eV and thus considerably closer to the LUMO of C_{60} (approximately 4 eV) than the workfunction of the Au electrode (approximately 5.1 eV) used by Ben-Sasson.

gives strength to the argument of Ben-Sasson *et al.* that more and larger openings in the source electrode are desirable as they remove the dependence of transistor operation on this supercapacitor concept.

Indeed, Ben-Sasson *et al.* have provided a very thorough explanation of the working principles of the OSBT based on experiments and simulation alike (see figure 3.7) [203,209]. According to this description, the Off-state of an OSBT is dominated by leakage currents from the top surface of the source electrode, which may not be controlled by the gate field due to screening effects. This Off-state current may be described as an injection-limited current (with injection barrier Φ_B) of the form

$$I_{Off} = e\mu N_0 F_\perp \exp\left[-\frac{e\Phi_B}{k_B T}\right](1 - FF) \tag{3.3}$$

where N_0 is the density of states in the active layer, $F_\perp$ is the perpendicular source-drain field at the top surface of the source electrode and the factor $(1 - FF)$ accounts for the fact that only the top surface of the source contributes to the leakage currents, while injection from the openings (with fill-factor FF) is switched off by the gate. These openings may in fact be treated similar to a coplanar, bottom-gate OFET (see figure 2.1): As the gate potential is increased, it serves to weaken the injection barrier of the vertical sidewalls of the openings and charges are injected into the semiconductor. In analogy to the OFET picture, they are pulled towards the gate dielectric interface inside the opening and accumulate there. As they cannot diffuse further than the diameter of the opening, the accumulated charges form a *virtual contact* at the bottom of the opening. Since the source-gate field and the source-drain field act against each other, a 'tunnel' of almost zero field-strength forms at the sidewalls of the opening, and - depending on the diameter of the opening - this effect may even extend into the centre of the opening. Consequently, charge carriers from the virtual contact diffuse, rather than drift, towards the drain until they reach the inversion point above the source electrode at which the source-gate field and source-drain field stop cancelling each other out. From the inversion point onwards, charge carrier transport towards the drain is drift-dominated. The position of this inversion point depends upon the thickness of the source electrode[2]. The drift-dominated On-state

[2] Ben-Sasson *et al.* have studied the effects of source electrode thickness, opening diameter, fill-factor, injection barrier height and dielectric thickness upon the performance of the OSBT and derived optimisation rules from these results [203].

current, according to Ben-Sasson *et al.* must then take the shape of a space-charge limited current with

$$I_{On} = \frac{9}{8}\varepsilon_0\varepsilon_r\mu\frac{V_{DS}^2}{L^3}FF \tag{3.4}$$

where L is the effective channel length.

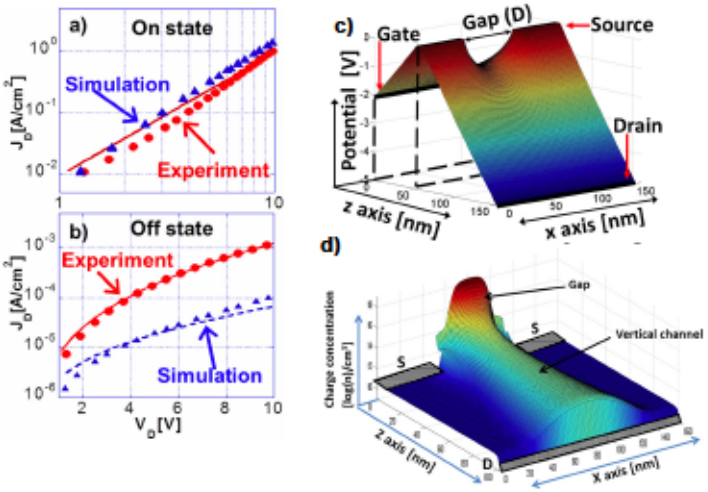

Figure 3.7.: Working mechanism of the OSBT as proposed by Ben-Sasson *et al.*: (a) Experimental and simulated On-state current of the OSBT with fit lines, (b) Experimental and simulated Off-state current of the OSBT with fit lines, (c) Simulated potential distribution in the On-state and (d) charge carrier distribution in the On-state. Reprinted from ref. [203] with the permission of AIP Publishing.

Chen *et al.* have described the OSBT operational mechanism for the special case of CNT or graphene source electrodes [210, 211]. These must indeed be considered separately due to the unique properties of the source materials in question. Chen *et al.* showed that application of a gate field not only narrows the Schottky barrier due to band bending (as is the case for metal electrodes) but also modulates its height. This latter effect is possible because of the significantly lower DOS in these materials in comparison with metal electrodes. For the case of CNT electrodes, the authors suggest that the Off-state current is dominated by thermionic emission over the Schottky barrier, while the On-state current is dominated by a strong tunnelling component through the thinning Schottky barrier. Consequently, the On/Off ratio can be improved by suppressing the thermionic component with a higher Schottky barrier, while enhancing the tunnelling in the On-state through narrowing of the barrier [211]. Chen *et al.* further argue that the gate effect can be enhanced if the CNT electrode is prepared such that it consists primarily of thin CNTs, ideally in a monolayer, since stacks of CNTs would increase the screening effect.

The same is true for graphene electrodes, where a thin graphene sheet is preferable to several graphene layers. Furthermore, a large number of holes in the graphene is beneficial for operation according to the simulation, while the hole diameter should be kept small to avoid screening of the gate from the channel layer [210]. According to the authors, the improvement in graphene-based OSBT performance observed by Lemaitre *et al.* in comparison to the previous CNT-based OSBTs is due to the fact that the continuous graphene sheet allows for more precise control of the injection barrier, since barrier lowering and narrowing take place only in the perforations, where they are desirable.

So far, research into OSBTs, both experimental and theoretical, has concentrated on the structure and operation of the source electrode. If contact doping (e.g. by a suitable SAM [212]) were included and the devices optimised for integrated circuit or high-frequency applications, it is to be expected that OSBTs would prove promising candidates for low-cost, large-area applications of organic electronics.

3.3. VERTICAL ORGANIC FIELD-EFFECT TRANSISTORS (VOFETS)

The vertical organic transistors discussed so far all have a common feature despite their obvious differences in working mechanism: Charge carrier transport is strictly vertical. While this approach certainly offers the potential for extremely short transport paths, high current densities and, from an application point of view, high integration densities, it also comes at a certain cost: The easy manufacturing processes and simple geometries do not necessarily allow for much design freedom. Insulation of the base electrode in standard OPBTs for example is not so easily realised and contact doping for the source electrode of OSBTs is only possible if a suitable SAM is available, since molecular doping of the vertical sidewalls in the openings is difficult.

In 2003, Stutzmann *et al.* and Parashkov *et al.* proposed a slightly different device concept, which operates on both horizontal and vertical transport and thus unites the design freedom of conventional OFETs with the short channel lengths of vertical transistors [213, 214]. These devices were later termed VOFETs [170] in order to highlight their strong resemblance of a conventional OFET. As with OPBTs and OSITs, there are essentially two sub-categories to this class and they shall be discussed separately in the following, as their geometries and working mechanisms are not exactly identical.

3.3.1. STEP-EDGE VOFETS

The transistors proposed by Parashkov *et al.* and Stutzmann *et al.* fall into the category of step-edge VOFETs, a term coined several years after their first demonstration by Takano *et al.* As the name suggests, the key feature of this geometry is the wrapping of the transistor channel around some kind of vertical edge, which acts as a spatial separator between the source and the drain electrode, as can be seen from figure 3.8. The gate electrode generally follows this edge, so that the entire channel length has a gate dielectric interface similar to that in conventional OFETs. As a consequence, the operation mechanism of this structure is perhaps best described as that of a short-channel OFET: In the On-state, charge carriers are emitted more easily from the source electrode due to the Schottky barrier narrowing provided by the gate field. The carriers consequently pass the bulk of the semiconductor in order to accumulate at the gate dielectric interface. Diffusion along this interface now results in transport in the vertical direction and so the charge carriers are eventually collected by the drain field which may be located above or underneath the source electrode. Similarly, the gate field suppresses charge carrier injection in the Off-state, so that only a weak leakage current between source and drain is measured here, which depends largely on the insulation properties of the step-edge.

While both Parashkov and Stutzmann used a VOFET design which relies on a polymer insulating layer between the otherwise overlapping source and drain electrodes - an approach also favoured by Yutani *et al.* [215] and Liu *et al.* [216] - later works often separated the source and drain not only in height, but also by a lateral distance so as to reduce leakage currents. This idea was first introduced by Chen *et al.*, who used a pre-patterned silicon substrate as the step-edge template for their device. In a similar fashion, Naruse *et al.* created a step-edge by pre-patterning the gate and dielectric layer on a planar substrate to a step-edge height and equivalent channel length of only 100 nm [217], which is still the shortest channel length ever reported for a step-edge VOFET. Accordingly, their device showed a clear contact limitation and the onset of an SCLC regime at high drain voltages (see figure 3.9). As already pointed out by Parashkov *et al.* and Stutzmann *et al.*, precisely this behaviour would be expected of a short-channel OFET. It should therefore be considered as first experimental evidence that VOFETs are indeed governed by the same operational principles as conventional OFETs. Naruse *et al.* consequently made slight changes to the expression for On-state current developed from the gradual channel

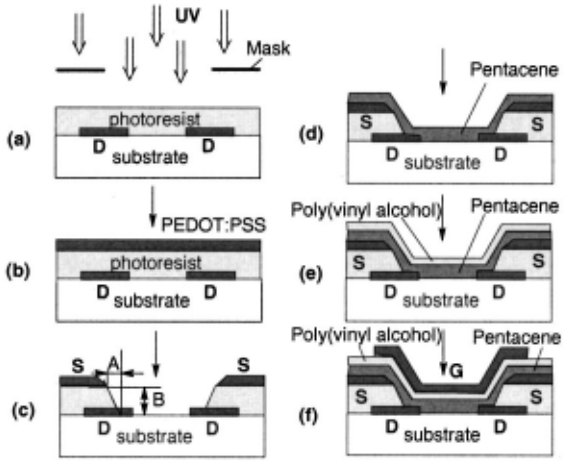

Figure 3.8.: The preparation process of the step-edge VOFET proposed by Parashkov *et al.* (a) Borosilicate glass substrate with patterned drain electrodes covered with a 1.4-µm-thick photoresist film is exposed to UV through a mask. (b) The source electrodes are applied perpendicular to exposed areas above the drain contacts, and channel widths are controlled by the width of the source electrodes. (c) Vertical drain–source channel is formed by development of the photoresist (A=2 µm, B=1.4 µm), and channel lengths were calculated as 2.4 µm. (d) Pentacene active layer evaporation. (e) Poly(vinyl alcohol) dielectric layer spin-coating. (f) Gate deposition above vertical drain–source channel. Reprinted from ref. [213] with the permission of AIP Publishing.

approximation (see equ. 2.2 and 2.3) and thus presented an analytical expression for the On-state current of their device.

More recently, two groups have considerably advanced the technology of step-edge VOFET fabrication, namely the group of Prof. Kudo at Chiba University and the group of Prof. Takeya at Osaka University. Prof. Kudo's group has successfully demonstrated that a step-edge may be produced also by depositing a sufficiently thick gate electrode [218] and were thus able to achieve step sizes of 0.5 µm [219] and On/Off ratios of 10^4, with cutoff frequencies just reaching the MHz regime [220]. The group of Takeya, starting with a comparatively low performance p-type device [221] has developed several slightly different architectures for both rigid [222–224] and flexible substrates [225–227], which are all based on the general idea of forming a step-edge already on the substrate, either by patterning a silicon wafer [222, 223] or by forming a step-edge on a flat substrate using epoxy or photoresist [221, 224–227]. The p-type VOFETs fabricated in this manner generally show a weak saturation regime or no saturation regime at all, depending on the height of the step [223, 225]. In the case of very thin steps of < 1 µm length, they also begin to present a certain amount of contact limitation, high-lighting once more the short-channel OFET

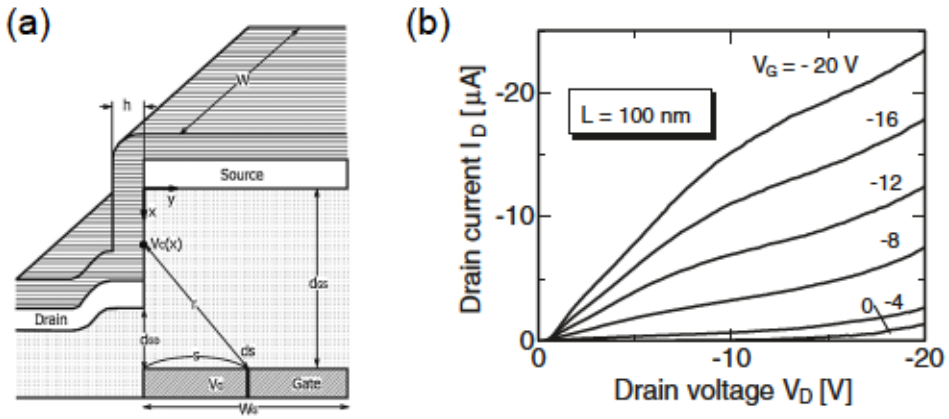

Figure 3.9.: (a) Schematic representation of the step-edge VOFET of Naruse *et al.* and (b) output characteristics of this device. Reprinted from ref. [217] with permission from the Japan Society of Applied Physics (JSAP).

nature of these devices. By gradually optimising the processing conditions to realise smaller electrode overlap, better molecular orientation in the vertical channel and shorter channel lengths, Uno *et al.* have recently managed to fabricate a p-type step-edge VOFET based on DNTT which shows an On/Off ratio of 10^7, which is the highest On/Off ratio of vertical organic transistors reported to date. Furthermore, they have implemented these step-edge VOFETs into a rectifying circuit which operates above 20 MHz and is thus more than sufficient to be used in RFID technology (operation frequency here is 13.56 MHz) [224].

Unfortunately, a comprehensive theoretical study on the precise operating mechanism of step-edge VOFETs has not been presented yet, so that the general operating mechanism must be estimated from the experimental data discussed above. The similarity of the layer stacks around the source electrode leave no doubt that the injection behaviour at least is indeed very similar to that of an OFET, as detailed in chapter 2. The further evidence for short-channel behaviour and contact limitation in both bottom- and top-contact step-edge VOFETs with step heights $\leq 1\,\mu m$ further suggests that an equivalent description by a short-channel OFET is at least a good approximation to describe the observed output characteristics.

3.3.2. THE NAKAMURA APPROACH

The step-edge VOFET concept has so far demonstrated both easy fabrication processes and excellent device performance for p-type VOFETs with standard high-mobility materials such as DNTT or Pentacene. This device concept however suffers from two major drawbacks: For one, the performance of these devices relies very much on the precise control of the processing conditions, as any misalignment during deposition of the source and drain electrodes can easily lead to large electrode overlaps or even short-circuits. This may severely limit reproducibility on a large scale. Furthermore, these devices are somewhat limited in design freedom, as for example the morphology of the semiconductor at the vertical sidewall may not be controlled so easily, nor can one deposit several different semiconductors into this channel. The implementation of the organic light-emitting transistor concept, for example, is thus not possible in a step-edge structure.

Assisted by Prof. Kudo, Nakamura *et al.* thus presented a different VOFET structure in 2006, precisely for the purpose of realising a vertical light-emitting transistor [228]. This device is perhaps best described as a conventional bottom-gate staggered OFET with OLED layers an additional contact stacked on top to realise a vertical architecture. Indeed, the authors were able to show that by insulating the top of the OFET contacts with a thick layer of SiO_2, they could inject holes into the semiconductor underneath the contacts which would then travel around the edge of the contact to enter the OLED stack, where they would recombine with electrons from the top drain electrode to produce light emission. A brief comment of the authors regarding the formation of the light-emission zone suggests that the vertical channel only gradually extends into the region between two source contacts, i.e. the lateral extend of this vertical channel appears to be a function of gate voltage. Nakamura *et al.* later improved upon the light emission behaviour of the device in order to realise a simple 16 x 16 Pixel display [229], but made no further attempt at investigating the precise transport physics of their device.

The concept itself, however, was recently taken up again by Kleemann *et al.* (see figure 3.11and it was shown that this simple structure may be used also for high-performance VOFETs with On/Off ratios of 10^6 [230]. As similar performances were obtained for both n-type and p-type devices (using C_{60} and Pentacene as active materials) with vertical channel lengths of 500 nm (for C_{60}) and 50 nm (for Pentacene), it was concluded that rather than being limited by the organic semiconductor, the performance of these devices

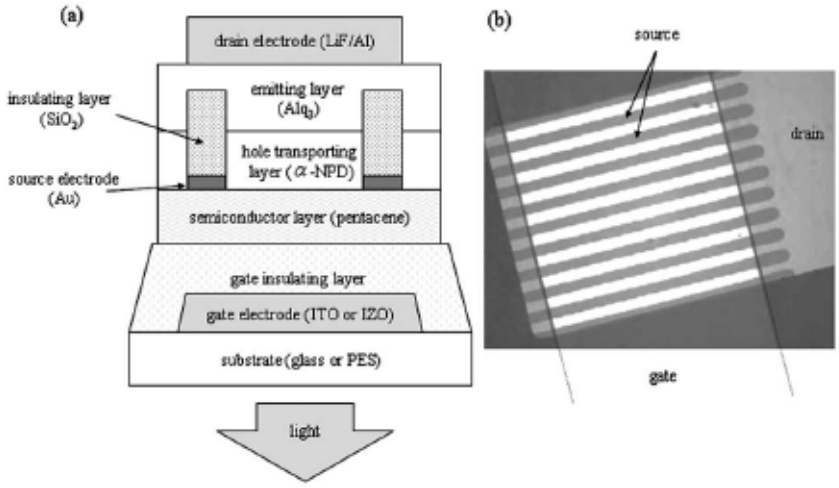

Figure 3.10.: (a) Schematic representation of the Nakamura VOFET and (b) a photograph of the real device under bias. Reprinted from ref. [228] with the permission of AIP Publishing.

must depend largely on injection (as typical for short-channel devices) and the quality of the structure. This, in particular, was improved considerably in comparison to the original device by Nakamura, as an orthogonal photolithography technique was used to structure the electrodes and insulator [90], which was assumed to produce cleaner and sharper vertical edges than the shadow masks previously used by Nakamura.

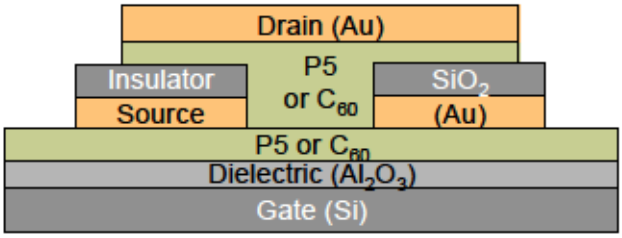

Figure 3.11.: Schematic of the VOFET proposed by Kleemann *et al.* [230] as a variation of Nakamura's approach.

Nevertheless, a full understanding of the working mechanism, as presented e.g. by Ben-Sasson for the OSBT, is currently missing for both step-edge VOFETs and the geometry of Nakamura. It is the aim of the subsequent parts of this thesis to use both experimental and simulation results in order to develop precisely such an understanding of the VOFET structure used by Nakamura and Kleemann. It is to be expected that these results, at least to a certain degree, may also be transferred to the step-edge geometry.

TECHNISCHE UNIVERSITÄT DRESDEN

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STUDY OF THE VERTICAL ORGANIC FIELD-EFFECT TRANSISTOR

4. METHODS AND MATERIALS

This chapter gives an overview over the materials and experimental methods used during the work for this thesis. After a brief summary of the electrical and chemical properties of semiconductors and dopants used within this work, the VOFET fabrication process will be discussed, including a discussion of structuring techniques suitable for patterning of organic electronic devices. Finally, the different methods used to characterise samples will be explained. Particular focus will be put on the transmission line method (TLM) and the method of electric potential mapping by thickness variation (POEM), which are essential and useful tools in order to determine the injection properties of transistors and the transport properties of organic semiconductors.

This chapter briefly discusses the materials and experimental methods used for sample fabrication and characterisation. For each of the materials used during device fabrication, chemical structures and the most important properties are summarised. Material deposition techniques, structuring methods and substrate preparation will be introduced only briefly and references to more extensive discussions will be given where appropriate. The characterisation methods used to investigate material and device properties will be discussed in more detail and particular focus will be given to the TLM analysis and the novel POEM concept, as much of the discussions following in later chapters build on results obtained with these two methods. Alternative methods to obtain such results will also be introduced briefly.

4.1. MATERIALS

The organic materials used to prepare the devices discussed in this thesis can be loosely categorised into matrix / transport materials and dopants. The properties of transport materials relevant for sample fabrication and measurements are summarised in table 4.1 with references to the field-effect mobility measurements, while suitable dopants for these materials are summarised in table 4.2. Two different oxide dielectrics as well as an organic insulator have also been tested during the work leading up to this thesis. Their most important properties are summarised in table 4.3. For completeness, the physical properties of the electrode materials used during device fabrication are provided in table 4.4. In each case, references for experimentally determined properties are provided.

Name	Abbreviation	Structure	Density [gcm^{-3}]	HOMO / LUMO [eV]	Mobility [cm^{2}V^{-1}s^{-1}]	Ref.
Pentacene	P5		1.325	5.1 / 3.2*	~ 0.5 (h)	[68, 104, 231, 232]
Dinaphtho-[2,3-b:2′,3′-f]-thieno[3,2-b]-thiophene	DNTT		1.473	5.4 / 2.4	~ 1.0 - 2.0 (h)	[233–236]
Buckminster-fullerene	C_{60}		1.630	6.4 / 4.0	~ 0.1 - 5.0 (e)	[90, 123, 237–239]
2,2′,7,′-tetra(N,N-ditolyl)aMino-spirobifluor	Spiro-TTB		1.280	5.25** / 1.9	~ 3x10^{-4} (h)	[240, 241]
Tris(8-hydroxy-quinolinato)-aluminium	Alq_3		1.325	5.8 / 3.8	1.4x10^{-6} (e)	[242, 243]

Table 4.1.: Physical and chemical properties of the transport materials discussed in this thesis. The hole (h) and electron (e) mobility values quoted here are field-effect mobilities measured in bottom-gate, top-contact OFETs with SiO_2 or Al_2O_3 as gate dielectric. HOMO and LUMO levels were determined by UPS. *Measured by Selina Olthof, IAPP. ** Measured by Martin Schwarze, IAPP.

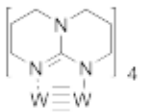
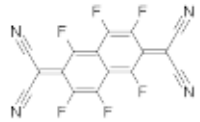
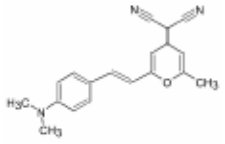
Name	Abbreviation	Structure	HOMO / LUMO [eV]	Type	Ref.
Tetrakis-(1,3,4,6,7,8-hexahydro-2H-pyrimido-[1,2-a]pyrimi-dinato)-ditungsten (II)	$W_2(hpp)_4$		2.4 / –	n-dopant	[244–246]
Dinaphtho-[2,3-b:2′,3′-*f*]-thieno[3,2-b]-thiophene	F_6-TCNNQ		— / 5.37	p-dopant	[29, 244, 247]
Fluorinated fullerene derivative	$C_{60}F_{36}$		— / 5.38	p-dopant	[29, 244, 248]
4-(dicyano-methylene)2-methyl6[p(di-methyl-amino)-styryl]4H-pyran	DCM		— / —	emitter	[249–251]
Molybdenum trioxide	MoO_3		9.70 / 6.70 *	p-dopant	[65, 252]

Table 4.2.: Physical and chemical properties of the dopant materials discussed in this thesis. *Energy level shift upon contact with air results in values of 8.5 / 5.2 [65].

Name	Abbreviation	Density [gcm^{-3}]	Relative permittivity	Ref.
Tetratetra-contane*	TTC	0.82	-	[85]
Silicon dioxide	SiO_2	2.60	3.9	[29, 244, 247]
Aluminium oxide	Al_2O_3	4.00	7.8	[29, 244]

Table 4.3.: Physical and chemical properties of the insulators / dielectrics discussed in this thesis. *Tetratetracontane ($C_{44}H_{90}$) is an organic molecule, its chemical structures is a long alkane chain and is therefore not displayed here.

Name	Abbreviation	Density [gcm^{-3}]	Work function [eV]
Gold	Au	19.3	5.1
Silicon	Si	2.3*	4.6 - 4.85*
Aluminium	Al	4.2	4.2
Silver	Ag	10.5	4.3

Table 4.4.: Physical and chemical properties of the electrode materials discussed in this thesis. Values for the work function were obtained by Selina Olthof, IAPP, using UPS. *Values taken from ref. [253]

4.2. SAMPLE PREPARATION

Apart from the VOFETs investigated in the remainder of this thesis, several other kinds of samples will be discussed also. For basic material characterisation, e.g. to investigate the morphology of certain organic layers or the electrical stability of insulators, a single layer of the material under investigation or a simple metal-insulator-metal (m-i-m) stack are sufficient, while transport properties of materials were investigated in OFET geometries and so-called p-i-p stacks (p-doped semiconductor / intrinsic semiconductor / p-doped semiconductor). The substrates and manufacturing techniques for these different kinds of samples are very similar and will briefly be summarised in the following paragraphs.

SUBSTRATES AND PASSIVATION

Two different kinds of substrates were used in the work discussed this thesis: m-i-m and p-i-p stacks were built on plain borosilicate glass substrates (supplier: Thin Film Devices, Inc.), while OFET and VOFET devices were built on silicon wafers (supplier: SIEGERT Wafer GmbH) which are p-doped with bromine so as to provide a conductive substrate (σ= 0.03 $\Omega^{-1}cm^{-1}$ - 1 $\Omega^{-1}cm^{-1}$). These wafers have a native SiO_2 layer and were subjected to a thermal or plasma-assisted atomic layer deposition (ALD) process [96] at the Institut für Angewandte Photophysik (IAPP, deposition done by Michael Sawatzki using PE-ALD), NamLab Dresden (deposition done by Claudia Richter, using thermal ALD) or Institut für Halbleiter- und Mikrosystemtechnik (IHM, deposition done by Dr. Christoph Hoßbach, using thermal ALD) prior to substrate cleaning and sample preparation. 30 nm of Al_2O_3 were deposited during these ALD processes, with very little variation in layer quality between wafers processed at IHM, NamLab and IAPP. Acting as the gate dielectric for OFETs

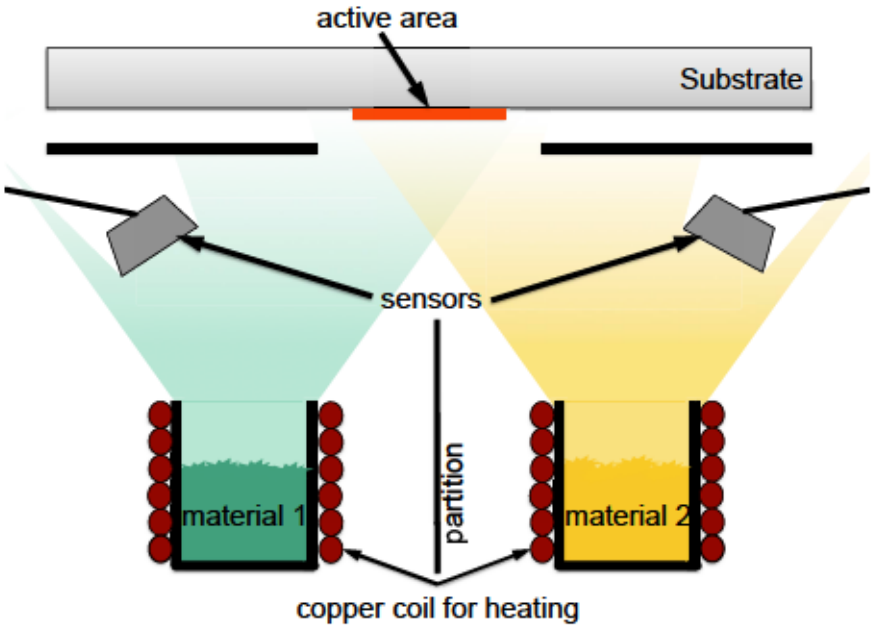


Figure 4.1.: Organic material deposition via thermal evaporation in a vacuum chamber. The thickness is monitored by individual QCM sensors for each material and the active area on the substrate may be defined by a photolithography mask on the substrate or a shadow mask, which may be placed inside the chamber or directly on the substrate.

and VOFETs, these layers provide a gate dielectric capacitance of (with $C = 0.23\,\mu F/cm^2$. Morphology studies were also performed on these dielectric-covered Si wafers, so as to ensure best comparability to actual transistor devices.

Prior to material deposition, all substrates were cleaned via immersion in acetone, ethanol and isopropanol and ultrasonication for 5 minutes each. To remove any further organic residuals on the substrate surfaces, the substrates were then treated in an oxygen plasma for 10 minutes. Si wafers were further immersed in hexamethyldisilazane (HMDS, Merck) for approximately 30 minutes directly before material deposition in order to passivate the dielectric surface. Residuals of HMDS were removed by a brief spin-rinsing step with isopropanol. The cleaned (and passivated) substrates were then directly transferred to a glovebox under nitrogen atmosphere or into vacuum in order to avoid further contamination.

4.2.1. PHYSICAL VAPOUR DEPOSITION

All materials were deposited under vacuum with a base pressure below 10^{-6} mbar. Organic

materials were evaporated[1] from aluminium nitride crucibles (supplier: CreaPhys) as illustrated in figure 4.1. These crucibles are surrounded by copper coils and thus heated via Joule heating, while the layer thickness and deposition rate can be monitored by quartz crystal microbalances (QCMs) placed above each source. The basic functional principle of these QCMs utilises the piezoelectric effect of the quartz [254]: The resonance frequency of the QCM changes with its mass, i.e. due to material deposition. This change in frequency is monitored and the gain in mass per unit area, m, calculated accordingly. If the QCM monitor is provided with the correct density ρ of the evaporated material, it provides the deposited layer thickness d from the relation $d = m/\rho$. The accuracy of a layer thickness reading is 0.1 nm and the sensitivity of a real-time deposition rate reading is 0.01 nm/s. Prior to sample fabrication, QCMs must be calibrated so as to give a correct reading of the layer thickness deposited on the substrate. The so-called tooling factor, the parameter determined during calibration, states the ratio of material evaporated onto the measurement QCM and material deposited onto a reference QCM, which is placed in the sample position during calibration. As figure 4.1 further illustrates, mixed layers (e.g. of a matrix and dopant) may then be deposited by co-evaporation of the two materials in question, with separate QCM monitors for each material.

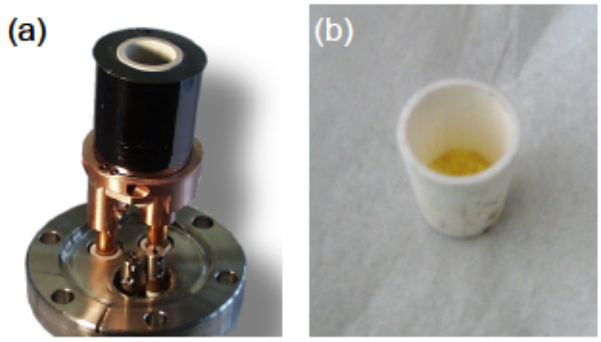


Figure 4.2.: Images of a complete evaporator unit (a) and crucible (b) filled with organic material. Pictures by Christian Körner, IAPP

Metal deposition for electrodes, as well as deposition of the p-dopant MoO_3 can be done in a similar fashion, i.e. by thermal evaporation from a crucible with deposition monitoring via QCMs. For the deposition of Au, Ag and MoO_3, a thin tungsten or molybdenum crucible may be used, which is directly connected to a power source. In the case of Al, a boron

[1] Many organic materials sublime upon heating in vacuum, but there are also others which melt and then boil. For simplicity, both processes will be referred to as evaporation here as the exact process makes no difference for the further discussion.

nitride crucible has to be used, so as to prevent diffusion of melted Al through the crucible.

A special case is the deposition of the source insulator in VOFET geometries. As will be discussed in more detail in chapter 5, SiO_2 is difficult to deposit via thermal evaporation from a crucible. The source insulator layer for VOFETs was therefore deposited via radio-frequency magnetron sputtering [255, 256] with Argon as the process gas. Again, deposition conditions were monitored using a QCM.

DEPOSITION SYSTEMS

Two different kinds of evaporation systems were used to produce samples: Two of the IAPP's multi-chamber systems, referred to as UFO I and UFO II, and two single-chamber systems (Kurt J. Lesker company), referred to as Lesker A and Lesker B. In the multi-chamber systems, deposition of metals, intrinsic, n-doped and p-doped layers can be done in separate vacuum chambers. These usually have a base pressure of 10^{-7} mbar and are connected to a larger central chamber via valves, which are closed during evaporation to avoid contamination of the entire system. The central chamber also contains a remote-control sample handling system, samples can consequently be transferred between chambers without contact to air. Substrates in this system are limited to a size of 2.54 x 2.54 cm^2.

The single-chamber systems also have a base pressure of 10^{-7} mbar and are operated by technical staff. The substrate, which may be as large as 15.24 x 15.24 cm^2 (giving a wafer of 6 x 6 samples of the smaller substrate size), is rotated horizontally during evaporation so as to produce a more homogeneous layer thickness. The system further contains partial shutters so as to allow for the controlled deposition of materials on certain rows or columns of the 6 x 6 wafer. This feature was utilised for the p-i-p devices in order to "wedge" the layer thickness of intrinsic layers.

Both single-chamber and multi-chamber systems are connected to glove boxes under nitrogen atmosphere, a transfer to other glove boxes or measurement setups without contact to air was thus possible by transporting samples in air-tight containers. This is particularly important as most of the sample layouts discussed in this thesis were non-standard layouts and samples could thus not be encapsulated by the normal procedure of IAPP[2].

[2] Encapsulation is done by glueing a glass cavity over the active area using the UV-cured resin XNR5590 (Nagase). A moisture getter (Dynic) may be inserted into the cavity to avoid degradation by water diffusion. This encapsulation procedure was only possible for p-i-p devices, as these were fabricated in the standard encapsulation-compatible layout.

4.2.2. STRUCTURING METHODS

Many organic electronic devices require some form of structuring technique in order to pattern electrodes, dielectrics or the organic layers themselves. One way to pattern a layer in a thermal evaporation process is shown in figure 4.1: By placing a shadow mask close to the substrate surface, only parts of the substrate are exposed to material vapour during deposition. This structuring technique can be applied to any kind of thermally evaporated material and may also be used to structure layers on top of organics. The resolution of this structuring method depends on the quality of the mask and its distance to the substrate surface, but is generally believed to be too poor for fabrication of high-performance OFETs, as the minimum achievable channel length is usually in the order of several micrometers. Furthermore, the edges of e.g. contact pads which were structured this way is generally rather unsharp, making an exact determination of the channel dimensions even more difficult. For the preparation of simple vertical stacks however, such as OLEDs or the p-i-p devices discussed in this thesis, shadow masks provide a simple structuring method of sufficient accuracy. The shadow masks available in the Lesker evaporation systems (mounted in the chamber underneath the sample holder) were therefore used to pattern p-i-p devices for POEM measurements as well as m-i-s capacitor stacks which will be discussed in chapter 8. The resultant device layouts on 2.54 x 2.54 cm^2 samples are shown in the top half of table 4.5. In a similar fashion, m-i-m stacks were structured in the multi-chamber evaporation systems. Here, shadow masks for 2.54 x 2.54 cm^2 substrates were mounted directly onto the sample holder before moving the sample into vacuum. The resultant device layout is similar to that shown for p-i-p devices.

For the fabrication of OFETs and VOFETs, a patterning technique is required which not only works on top of organic materials, but also provides small feature sizes and clearly defined vertical edges. For this reason, the source and drain electrodes in these devices, as well as the source insulator for the VOFET, were patterned using a novel bi-layer photolithography process (see figure 4.3). The novelty of this approach lies in the combination of a conventional imaging resist with a protective lift-off resist. As few organic materials are compatible with the solvents and developers commonly used for conventional imaging resists (e.g. NaOH or toluene), photolithography is not normally possible on top of organic layers. To circumvent this issue, DeFranco *et al.* developed a highly fluorinated resist which is benign to most organic materials. Solvent and developer

compounds for this resist are also highly fluorinated, such that the resist may be used as a protective layer between a conventional imaging resist and an organic material. DeFranco *et al.* further demonstrated that their resist may also be used as a stand-alone negative imaging resist if combined with a photo-acid generator (PAG) [257–259].

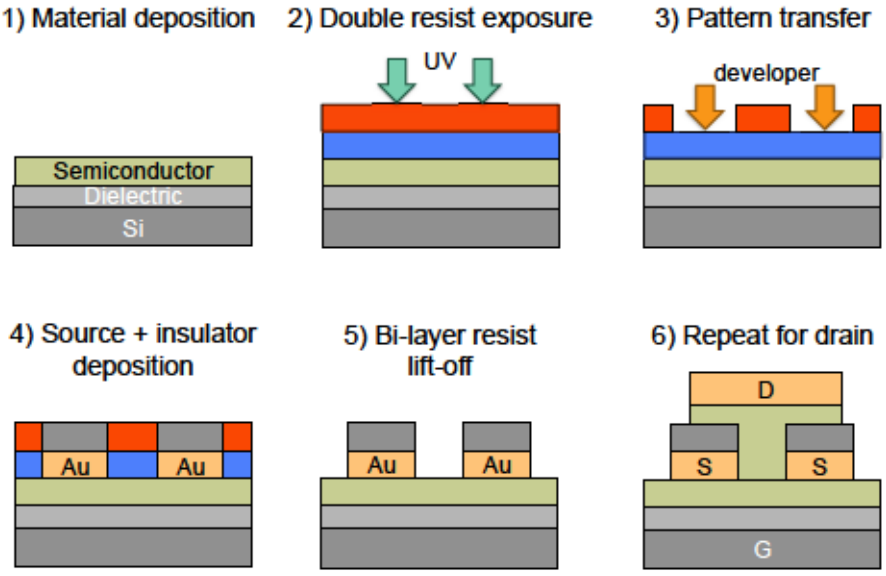


Figure 4.3.: Schematic representation of the bi-layer photolithography process. The protective and lift-off resist Ortho 310 is shown in blue, the imaging resist ma-P 1210 is shown in red.

In the work leading to this thesis, a PAG-free version of the resist developed by DeFranco *et al.*, referred to as Ortho 310 (available from Orthogonal, Inc.), was used as the protective and lift-off resist in the bi-layer photolithography approach previously described by Kleemann *et al.* [90, 260]. Electrodes for OFETs and VOFETs were thus patterned by spin-coating *Ortho 310* onto the active layer (i.e. the organic semiconductor) at 3000 rpm for 30 s, followed by a post-application bake (PAB) of 5 minutes at 80 °C. The positive imaging resist *ma-P 1210* (micro resist technology GmbH) was spin-coated on top of this protective layer, also at 3000 rpm for 30 s, and baked for 1 minute at 80 °C. The thickness of each layer after this procedure is approximately 1 µm. The imaging resist was exposed to spectral light (313 nm, 365 nm, 405 nm) for 2 - 4 s (depending on the substrate conditions) using a maskless *SF-100* exposure tool (Intelligent Micro Patterning) with a mercury lamp, micro-mirror array and additional lens. The additional lens produced an exposure field of 3.7 x 2.7 mm^2 at a resolution of approximately 3 µm, allowing for the size of one OFET or VOFET contact mask (see lower half of table 4.5) per exposure and thus necessitating a step-by-step exposure of each substrate to produce several devices

per sample. The imaging resist was subsequently developed by dipping into in *ma-D 331* (micro resist technology GmbH) for 30 s and rinsing in de-ionised water (DI water). The pattern was then transferred to *Ortho 310* using a combination of puddle and spin etching with *developer 140* (Orthogonal, Inc.) and hydrofluoroether (*HFE 7100*, IoLiTec), where the exact etching protocol had to be adjusted to the surface roughness of the organic semiconductor / substrate and current ambient conditions (this will briefly be discussed in chapter 5). After contact metal and (for VOFETs) source insulator deposition, *Ortho 310* (and thus also *ma-P 1210* and the material deposited on top of it) was removed by an overnight lift-off procedure in *HFE 7100*, which was typically performed under nitrogen atmosphere. It has been shown by Zakhidov *et al.* that this process is harmless for most organic materials [258].

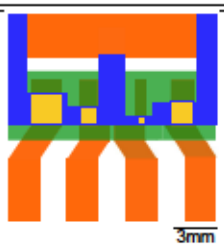
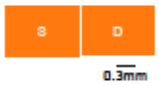
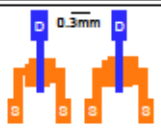
Device type	Layout	Mask type	Dimensions
p-i-p / m-i-m		Shadow mask	Active areas of 6.440, 3.265, 1.678 and 0.884 mm^2 , highlighted in light green
m-i-s*		Shadow mask	Active areas of 10.88 and 1.74 mm^2
OFET		Lithography	Channel width W = 1000 µm Channel length L = 25, 50, 100 and 200 µm
VOFET		Lithography	Channel width W = 600 µm (VOFET), L determined by layer thicknesses

Table 4.5.: Shadow and lithography mask structures used for patterning the samples discussed in this thesis. Different colours represent different masks for the same device. * m-i-s stands for metal-insulator-semiconductor capacitors, these will be discussed in chapter 8.

4.3. SAMPLE CHARACTERISATION

Due to the variety of investigated effects and the sample geometries necessary for these investigations, also a series of characterisation methods is required to gain a full

understanding of the processes that ultimately govern the VOFET's performance. The semiconductor morphology and exact device dimensions are investigated via suitable types of microscopes, while charge transport processes are investigated via electrical characterisation of full device stacks. This section briefly summarises the experimental methods used for this characterisation and also explains in more detail which type of device architecture is used for each individual analysis.

4.3.1. BASIC CHARACTERISATION METHODS

ATOMIC FORCE MICROSCOPY

Atomic force microscopy (AFM) was used to investigate the topography of organic film surfaces (mostly on Si wafers) so as to gain an understanding of the morphology of a specific material or blend layer and how it is affected by the substrate and processing conditions. As stated in chapter 1, the morphology of a film can greatly affect its electronic properties and is therefore an important and fundamental characteristic of any organic semiconductor film.

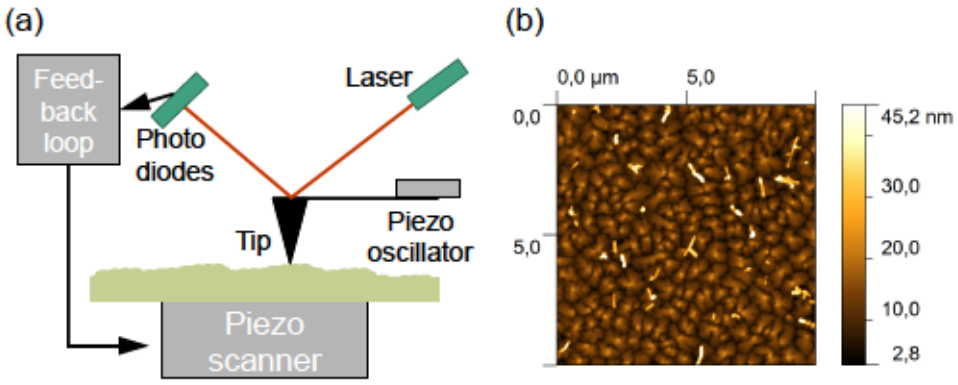


Figure 4.4.: (a) Schematic representation of the most important components of an AFM. (b) Exemplary topology of a 30 nm pentacene film on an Si wafer, obtained by Dr. Tobias Mönch (IAPP) using tapping mode AFM.

A simplified schematic of a standard AFM device is shown in figure 4.4 (a): The sample is scanned by a sharp silicon tip connected to a piezo oscillator. As the tip is brought in contact with the sample surface, its point and the molecules at the sample surface interact and lead to a deflection of the tip. This deflection is measured by reflection of laser light into a fast photo-diode and used by a feedback loop to control a piezo scanner and thus move the tip. To investigate the topography of an organic material, the AFM is operated in the so-called tapping mode (or intermittent contact mode), where the force of interaction

between tip and sample is smallest and thus least damaging to the organic material [261]. In this mode, the piezo oscillator drives the cantilever near its resonant frequency and Hooke's law is used to adjust the sample-tip distance such that the interaction force, and thus the oscillation amplitude of the tip, is kept constant.

For the AFM measurements presented in the following chapters, an *AIST-NT Combiscope1000* is used, which operates in ambient conditions. The silicon tip has a resonance frequency of approximately 300 Hz and scans are performed at a pixel rate of 0.1 s^{-1} and with an amplitude of typically 40 nm.

ELECTRON MICROSCOPY

Electron microscopes are used for a wide range of applications in physics, chemistry and biology. The general functional principle of these devices may be explained thus: An electron gun, mounted at the top of a vacuum chamber, produces a beam of electrons, which is accelerated to high energies (in the range of 1 keV - 300 keV) by an accelerator and then directed downwards through a series of condenser lenses. In scanning electron microscopy (SEM) [262], the condenser lens system is used to focus the electron beam onto the sample so as to investigate the sample surface. Information about the surface topography is obtained through secondary electrons, while material contrast is provided by backscattered electrons. In transmission electron microscopy (TEM) [263], a broad beam is directed through the sample[3]. Elastically scattered electrons in the transmitted beam give information about the morphology and structure of the sample. In both SEM and TEM, photon signals in the optical and x-ray range are also obtained through inelastic collisions. The x-ray signal may be used e.g. to perform energy-dispersive x-ray spectroscopy (EDX). In this method, the characteristic energy of x-rays produced by electron collisions with certain atoms is detected and used to gain information about the local chemical composition of the sample.

In the following chapters, planar and cross-sectional electron microscope images of the VOFET geometry will be presented, which were taken by Dr. Petr Formánek at the Leibniz Institut für Polymerforschung Dresden e.V. (IPF). Planar view images of the sample surface were recorded using a *Carl Zeiss NOEN40 EsB* or *Carl Zeiss Ultra55* SEM. The latter is equipped with a *Bruker Quantax XFlash5060* EDX spectrometer and was used

[3] This is possible only if the sample under investigation is very thin, typically on the order of 100 nm. In this case, however, TEM provides a considerably higher resolution than SEM.

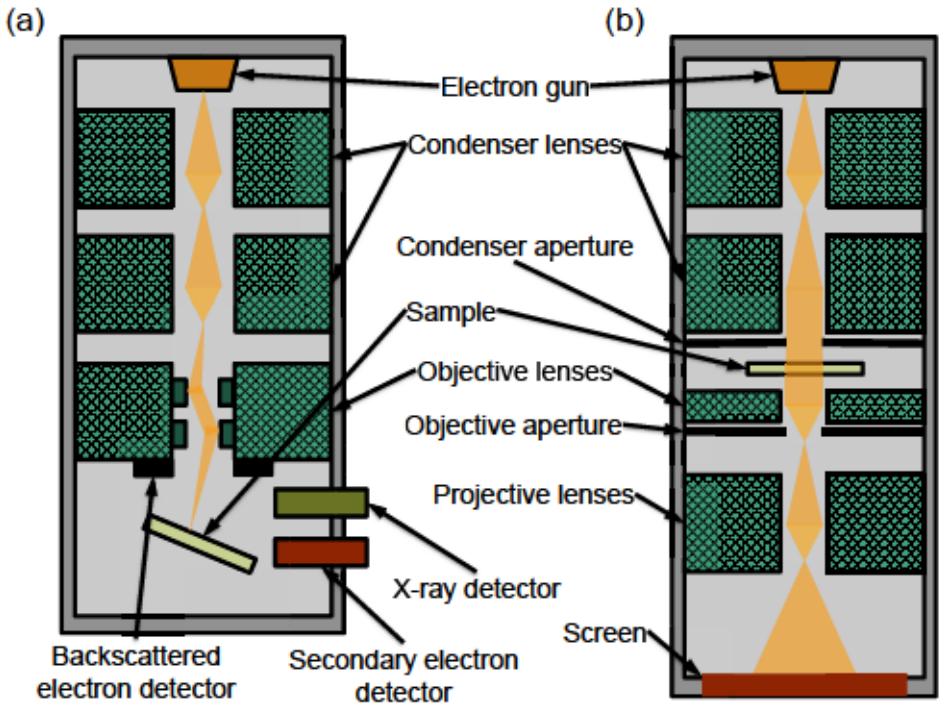


Figure 4.5.: Schematic representations of an SEM (a) and TEM (b). Orange rays denote the electron beam.

to obtain EDX spectra of the VOFET stacks at an electron acceleration voltage of 5 kV. Prior to these measurements, approximately 10 nm of amorphous carbon were deposited onto the samples in a *Leica EM SCD500* sputter coater to prevent charging during the measurement. Cross-sectional views of the VOFET stack were prepared by cutting a lamella of this stack with a focused ion beam (FIB) [264]. This was done by Michael Göbel (also of IPF), using a *Carl Zeiss NEON 40 EsB CrossBeam* SEM/FIB system. Prior to FIB cutting, the samples were coated with 30 nm of platinum (Pt) using the *Leica EM SCD500*. The lamella was then examined in TEM using a *Carl Zeiss Libra 120* electron microscope, which was operated at an acceleration voltage of 120 kV.

ELECTRICAL CHARACTERISATION

The electrical characteristics of OFETs and VOFETs were measured in a nitrogen atmosphere glovebox using a mechanical probe station with Au measuring tips mounted on micro manipulators for exact positioning on the devices' contact pads. The conductive silicon substrate was contacted by placing it on a copper plate. The copper plate and measurement tips of this setup are connected to a *HP 4145B* semiconductor parameter analyser containing two source-measure units (SMUs). During measurements, the source

contact of the OFET or VOFET was always kept at ground potential, while the gate or drain were swept at a rate of 0.1 V/s. In this manner, transfer and output characteristics of OFETs and VOFETs were obtained, from which several parameters can be extracted, as explained in chapter 2. A photograph and schematic representation of the contacted VOFET are shown in figure 4.6.

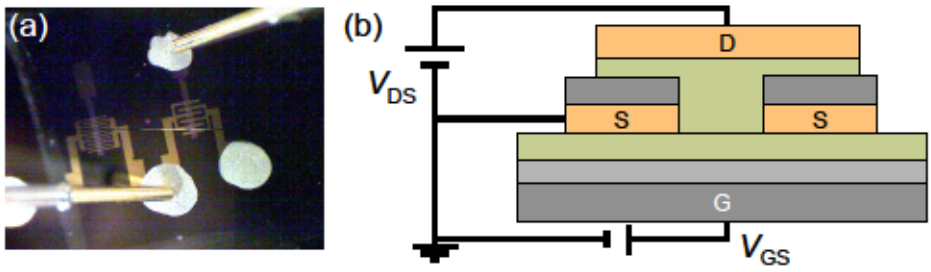


Figure 4.6.: Photograph and schematic representation of a VOFET during electrical characterisation.

The p-i-p devices used for POEM investigations (see section 4.3.3) were encapsulated (see section 4.2) and could thus be measured in ambient conditions using a *Keithley 2400* SMU.

4.3.2. TRANSMISSION LINE METHOD

The transmission line method, also referred to as transfer length method or simply TLM [265, 266], is a straight-forward approach to extract contact resistance from a series of transistors which are identical apart from a variation in channel length L. It was first developed by Luan and Neudeck to determine the contact resistance of amorphous silicon transistors [267] and has since then been used also in OFETs. Within the framework of this thesis, it will be used to discuss the effects of contact doping on both OFET and VOFET geometries (see chapter 7).

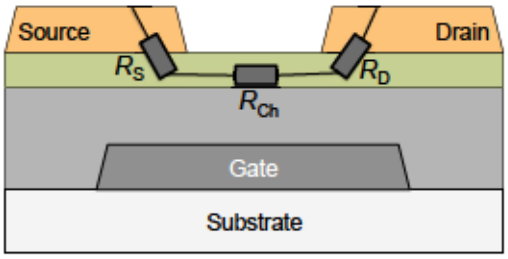


Figure 4.7.: Schematic representation of the series connection of R_C and R_{Ch} in a bottom-gate, top-contact OFET.

The total differential resistance of any given OFET, defined as

$$R_{OFET} = \frac{\partial V_{DS}}{\partial I_D}, \tag{4.1}$$

can be expressed as a series connection of contact and channel resistance (see figure 4.7), i.e.

$$R_{OFET} = R_{Ch} + R_C, \tag{4.2}$$

where $R_C = R_S + R_D$. The channel resistance is further given by

$$R_{Ch} = \frac{R_{Sheet}}{W} L, \tag{4.3}$$

where R_{Sheet} is the sheet resistance of the semiconductor in the channel region and W and L are the channel dimensions as defined before. Combining the above expressions, one finds that

$$R_{OFET} W = R_{Sheet} L + R_C W. \tag{4.4}$$

R_{OFET} can be extracted from the linear regime of the output characteristics of a transistor. Following equ. 4.4 with known L and W, it is therefore possible to extract R_C and R_{Sheet} as functions of V_{GS} for a specific material system from a series of identical OFETs with varying channel lengths by plotting the so-called width-normalised OFET resistance $R_{OFET}W$ versus channel length L for different gate voltages. This is illustrated in figure 4.8 for a pentacene OFET with Au top-contacts. Fitting equ. 4.4 to the obtained data, $R_C W$ and $R_{Sheet}$are given by the point $R_{OFET}W(L{=}0)$ and the gradient of the straight line fit.

Furthermore, an estimate of the gate voltage-dependent transfer length L_T (see chapter 2) can be extracted as the point where $R_{OFET}W = 0$, i.e.

$$L_T = \frac{L\left(R_{OFET}W = 0\right)}{2}. \tag{4.5}$$

While this method provides easy access to parameters such as channel resistance, contact resistance, transfer length or even mobility (extracted from the channel resistance [124]), it has certain drawbacks. Firstly, it is assumed that the channel sheet resistance is constant over the entire channel length. This may not be the case e.g. for devices contact-doped with relatively small molecules, where diffusion of the dopants may lead to changes in

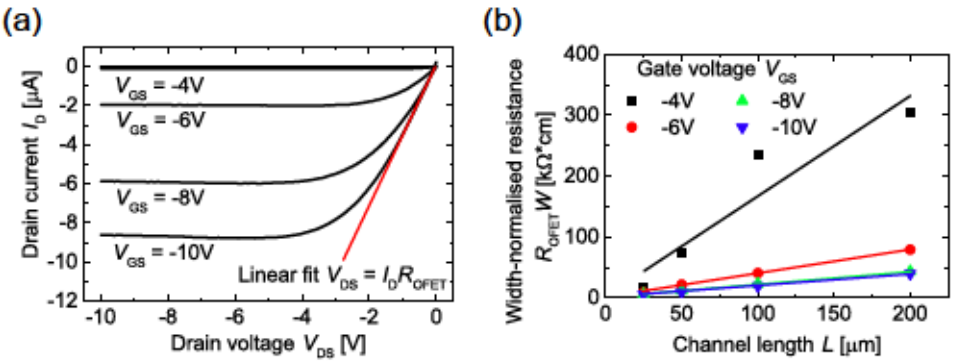


Figure 4.8.: (a) Output characteristics of an OFET with L = 25 µm and W = 1000 µm. The black line indicates where R_{OFET} is extracted using equ. 4.1. (b) $R_{OFET}W$ versus channel length for a series of bottom-gate, top-contact OFETs with pentacene as the active material and Au contacts. Straight lines indicate fits to equ. 4.4 for different gate voltages. Reprinted from the supporting information of ref. [268].

the sheet resistance near the contacts. It is further assumed that the apparent threshold voltage is independent of contact resistance. Especially in short-channel devices, this may not be the case, correct extraction of the gate-voltage-dependent mobility from the channel sheet resistance may therefore not be possible. Lastly, the accuracy of the method relies on the reproducible preparation of OFETs with varying channel lengths. Variations in the preparation conditions, semiconductor quality etc. can lead to strong inaccuracies in the TLM results and these typically play a bigger role in short-channel devices, where contact resistance is most prominent and should therefore be easiest to extract. Where necessary, these drawbacks may be overcome by using the modified TLM analysis developed by Xu *et al.* [269], which is less sensitive to parameter variation, or by reverting to some other method for extracting the contact resistance, such as four-probe measurements, Kelvin probe force microscopy or (for a very basic estimate, using only a single OFET device) the transition voltage method [270]. For the purpose of this work, however, the standard TLM analysis provides sufficiently accurate results, as will be discussed further in chapter 7. The application of other methods to extract contact resistance has therefore been omitted.[4]

4.3.3. ELECTRIC POTENTIAL MAPPING BY THICKNESS VARIATION

As illustrated in chapter 2 and in the previous section, a standard OFET geometry can be used to determine the lateral field-effect mobility of carriers in a given semiconductor

[4] Parts of this section were previously published in the supporting information to ref. [268].

material. The mobility determined in such a measurement is called the field-effect mobility and may differ strongly from the vertical bulk mobility of the material as it is found e.g. in OLEDs or OPV. A similar bulk transport may also be a relevant or even dominant mechanism in the VOFET architecture (this will be discussed further in chapter 6) and is thus investigated for the organic semiconductors used here.

The bulk mobility in organic semiconductors perpendicular to the substrate surface is often measured in a (single carrier) metal - intrinsic semiconductor - metal (m-i-m) or p-doped - intrinsic p-doped semiconductor (p-i-p) geometry (see figure 4.9 for a device schematic and exemplary characteristics). When applying a sufficiently high voltage to such geometries, one is able to observe an SCLC regime. By assuming a constant mobility independent of electric field F and charge carrier density n, along with trap-free, drift-only transport and ideal injection, one may extract the charge carrier mobility μ from the Mott-Gurney law [271]

$$j = \frac{9}{8}\varepsilon_r\varepsilon_0\mu\frac{V^2}{d^3}, \tag{4.6}$$

where ε_r is the relative permittivity of the semiconductor under investigation, ε_0 is the vacuum permittivity, and d is the thickness of the intrinsic semiconductor. Where the mobility is known to be field-dependent according to Poole-Frenkel dependence, one may instead use the Murgatroyd equation [272]

$$j = \frac{9}{8}\varepsilon_r\varepsilon_0\mu_0\frac{V^2}{d^3}\exp\left(0.891\gamma_{PF}\sqrt{\frac{V}{d}}\right), \tag{4.7}$$

where γ_{PF} is a temperature-dependent pre-factor derived from the Poole-Frenkel effect.

Without independent characterisation of the organic-metal interfaces however, it is unclear whether the above assumptions are valid in individual experiments. Here, a more accurate approach is provided by the method of electric potential mapping by thickness variation (POEM) [273]: By measuring the j-V characteristics of a series of m-i-m devices with varying intrinsic semiconductor thickness d (see figure 4.9), one is able to extract the driving voltage V required for a certain current density j as a function of d. It is possible to show that the voltage series $V(d)$ is equivalent to the potential distribution $\breve{}(x)$ in the intrinsic layer of the thickest device [273]. Thus it is possible to map the potential distribution across the thickest device by measuring also a series of thinner devices at the

same constant current density j. Once this potential distribution is obtained, it is straight forward to extract the electric field distribution

$$F(x) = \frac{\partial \Phi}{\partial x} \tag{4.8}$$

and charge carrier density

$$n(x) = \frac{\varepsilon_r \varepsilon_0}{e} \frac{\partial F}{\partial x}. \tag{4.9}$$

For drift-dominated transport, the field- and density-dependent mobility can then be directly extracted as

$$\mu_{SCLC}(x) = \frac{j}{en(x)F(x)}. \tag{4.10}$$

By performing this analysis for several different values of j, it is possible to determine any dependence of μ on n or F, i.e. one can directly map out $\mu_{SCLC}(F, n)$ from the measured j-V characteristics without assuming a specific transport model. A more detailed explanation of this approach may be found in ref. [273].[5]

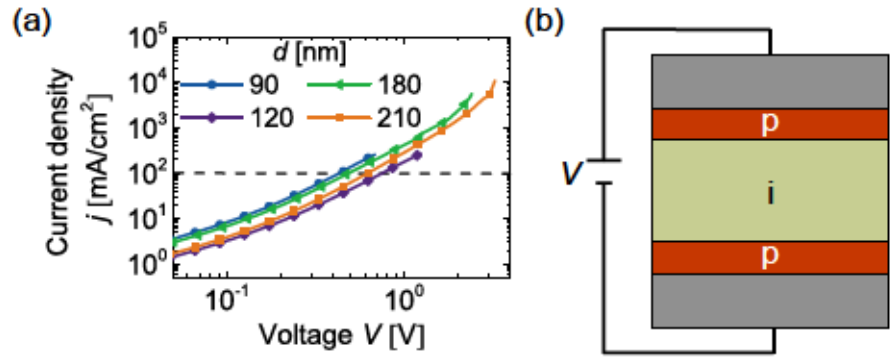


Figure 4.9.: (a) j-V characteristics of a series of p-i-p devices with varying thickness of the intrinsic layer. Reprinted from ref. [231]. (b) Schematic representation of a p-i-p device for POEM measurements.

P-i-p samples for the POEM method were produced in collaboration with Dr. Johannes Widmer (IAPP) and the above analysis was performed by him.

4.3.4. IMPEDANCE SPECTROSCOPY

Impedance spectroscopy is used frequently in organic electronics to investigate doping effects, trap distributions and charge carrier transport in diodes and other basic devices.

[5]Large parts of this section were previously published in ref. [231].

For the purpose of this thesis, a brief description of impedance spectroscopy, as it applies to purely capacitive elements, will be given. For a more extensive discussion of this matter, the interested reader is referred to ref. [274].

The fundamental principle of impedance spectroscopy is to monitor the current response of a given device to an applied DC voltage V_{DC} which is superimposed by a small AC voltage signal V_{AC} oscillating with an angular frequency ω, such that

$$V(t) = V_{DC} + V_{AC}\sin(\omega t). \tag{4.11}$$

The current response of the device will be phase-shifted by φ, determined by the type of device:

$$I(t) = I_{DC} + I_{AC}\sin(\omega t + \varphi). \tag{4.12}$$

By measuring the current response over a large frequency range it is possible to identify different physical phenomena, such as charge carrier injection, trapping, transport and dielectric relaxation, on the basis of their characteristic time constants. The complex impedance of this device is given by

$$Z = \Re(Z) + \Im(Z)\hat{i}, \tag{4.13}$$

where the real and imaginary parts are defined as

$$\begin{aligned}\Re(Z) &= \frac{V_{AC}}{I_{AC}}\cos(\varphi)\\ \Im(Z) &= \frac{V_{AC}}{I_{AC}}\sin(\varphi).\end{aligned} \tag{4.14}$$

For a purely capacitive device, the phase shift is φ = -90°, consequently the real part of Z is zero and the imaginary part gives the device's capacitance C as

$$\Im(Z) = -\frac{1}{\omega C}. \tag{4.15}$$

The response signal of such a capacitive device is shown in fig. 4.10, with capacitance values calculated using equ. 4.15[6].

[6]The occurrence of a single plateau clearly indicates dielectric relaxation behaviour, other processes would manifest themselves as additional plateaus in a *C-f* plot.

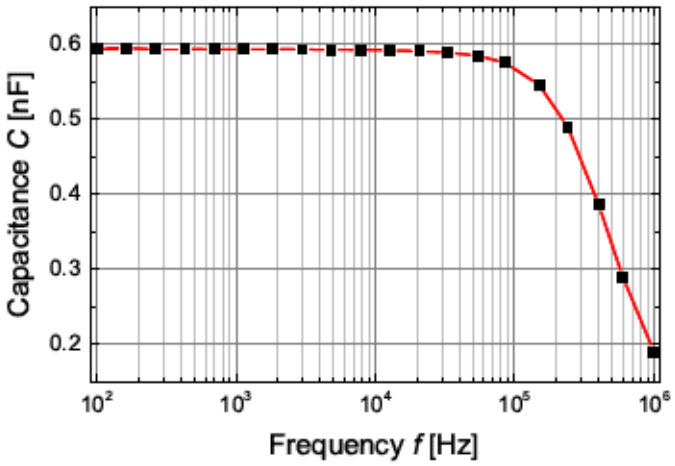


Figure 4.10.: Exemplary *C-f* curve of a capacitive device, in this case an m-i-m structure made of aluminium contacts and a polymeric insulator.

In chapter 8 of this thesis, this analysis will be used to discuss the accumulation / depletion behaviour of thin dopant layers in metal-insulator-semiconductor structures under varying DC bias (this is referred to as capacitance voltage spectroscopy). Samples for this analysis were measured in a nitrogen glovebox using the same probe station as for *I-V* characteristics of transistors. As measurement device, an *AUTOLAB PGSTAT302N* galvanostat was used, which measures impedance by a lock-in amplifier in the range of 1 µHz to 1 MHz and with DC bias between 0 V and ±8 V.

5. MATERIAL OPTIMISATION FOR VOFETS

This chapter presents and discusses results obtained during the very first experiments on VOFETs after the initial publication of this device structure. It is intended as an introductary chapter to the results part of this thesis. By describing a series of smaller experiments which in themselves were not profound enough for publication in a journal, the chapter aims to discuss some of the experimental difficulties involved in VOFET fabrication, which in turn lead to a first, very basic understanding of the operational principle of the VOFET. This chapter thus forms the basis for the following chapters, in which these operational principles will be analysed in more detail.

When the photolithographically patterned VOFET was first published by Kleemann *et al.* in 2013 [230], very little was known about its fundamental operational principles and also about the processing parameters which would most affect performance. While the ultimate aim of this thesis is to give a detailed explanation of the operational principle of the VOFET, this chapter will first of all discuss the dependence on processing parameters, so as to allow the reader to reach an understanding of the VOFET geometry in a somewhat "top-down" approach and to follow the chronological path to the development of this understanding. This chapter, therefore, will analyse the fabrication process of VOFETs in more detail and highlight two important processing aspects which strongly affect the VOFETs performance: The deposition of a suitable source insulator and the morphology of the active semiconductor layers.

Beginning with a discussion of the insulator deposition process chosen by Kleemann *et al.* and suggesting alternative methods and materials, the effects of semiconductor morphology variations will then be analysed and first ideas regarding charge transport in the VOFET will be presented, so as to lay the groundwork for the next chapter, in which this topic will be discussed in detail.

5.1. VARIATION OF THE SOURCE INSULATOR

Kleemann *et al.* fabricated the first photolithographically patterned VOFETs by depositing either 25 nm of pentacene or 40 nm of C_{60} onto a HMDS-treated Si substrate, forming a lithography mask on top of this organic layer and depositing 35 nm of Au as the source electrodes and 100 nm of SiO_2 through this mask via thermal evaporation and RF magnetron sputtering (see chapter 4 for details). VOFETs were finished by lifting off the first photolithography mask, replacing it by a second mask and depositing another 25 nm of pentacene or 460 nm of C_{60} through this second mask, followed by a drain electrode made of 35 nm Au. This second mask, too, was lifted off in HFE to finalise the devices.

While this procedure was successfully employed to demonstrate working VOFETs, it is easy to see that a high-energy deposition process such as RF magnetron sputtering might produce a certain amount of problems when used on top of a sensitive organic material such as the semiconductor or the heat-sensitive resist layers. And indeed, the yield of these first VOFET devices was often found to be very poor due to failing

lift-off procedures. Figure 5.1 (b) illustrates one of the most common issues with lift-off procedures in this VOFET geometry: The impact of high-energy ions on the surface of the photoresist, perhaps combined also with the UV radiation emitted by the argon plasma during sputtering, damages the photolithography mask in a way that strongly reduces its solubility in HFEs and even in stronger solvents such as acetone. This is particularly problematic when depositing thin source electrodes made of Au, as the cluster-like growth of which increases the probability for local heating during sputtering due to the bad heat conductivity between Au clusters[1]. Depositing thicker layers of 50 nm Au to allow for a more homogeneous distribution of thermal energy during sputtering partially circumvents this issue. In subsequent experiments, the thickness of the source electrode is therefore always set to 50 nm.

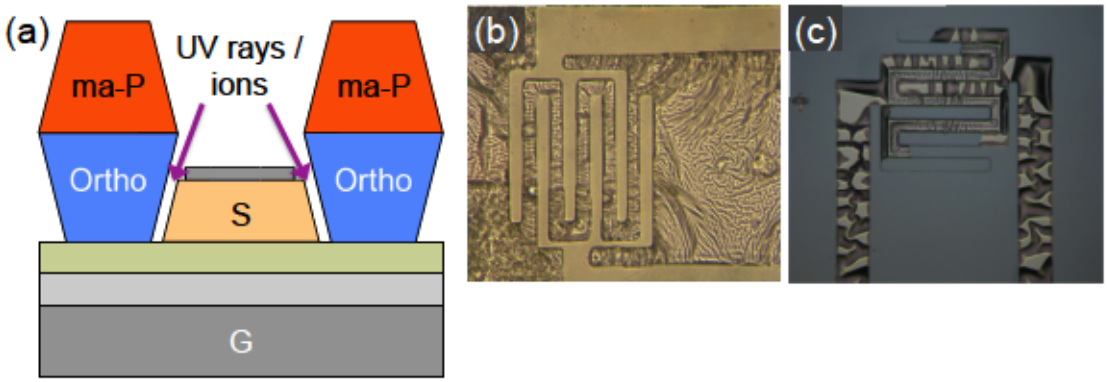


Figure 5.1.: (a) Schematic representation of a VOFET sample during deposition of the source insulator by sputtering. (b) Optical microscope image of a VOFET sample after the first lift-off step in HFE, where the lift-off failed due to increased insolubility of the Ortho resist. (c) Optical microscope image of a VOFET sample after the first lift-off step in HFE, where the source electrode has partially been lifted due to large quantities of Ortho resist underneath the Au.

Another negative effect of the sputtering process is highlighted in figure 5.1 (c): Damage of the undercut edges of the lithography mask may lead to a collapse of these edges. This was found to be more likely the larger the undercut is to begin with, i.e. the effect also depends on the processing parameters during photolithography. The collapse of these undercut edges is believed to lead to an increased diffusion of the Ortho resist underneath the source electrodes, so that the HFE solvents employed during lift-off may lift off not only the lithography mask - as intended - but also the source contacts by dissolving the Ortho resist underneath them. Depending on the strength of this effect, the source may

[1]This manifests as bubbles in the resist layers which are visible even with the naked eye.

only partially be lifted. This consequently produces the wave-like topography of the source contact shown in figure 5.1 (c)[2].

In addition to the difficulties found during lift-off procedures, it can also be shown that the sputtering process is potentially harmful to the active semiconductor layer underneath the source electrode. To demonstrate this, the VOFET fabrication process is stopped after the first lift-off procedure. Using the two adjacent source contacts as the source and drain electrodes for a conventional OFET with L = 50 µm and W = 2500 µm (the length and width of the OFET channel as given by the width and separation of the two VOFET source contacts, see table 4.5), one can measure directly the field-effect mobility of the pentacene layer after the sputtering process. Figure 5.2 shows the transfer and output characteristics of such an OFET measurement of an incomplete VOFET structure. A reference device with the same dimensions and materials, but without the layer of sputtered SiO_2 on top of the contacts, is also shown and measurements were performed after lift-off. It is obvious from this comparison and the extracted performance parameters (see table 5.1) that the sputtering process does indeed damage the underlying pentacene layer in such a way that a lower effective mobility is determined for the SiO_2-covered sample.

In order to ensure the best possible VOFET performance, it seems necessary to determine if and to what extent damage of the lower pentacene layer is relevant for this performance, i.e. to what extent the lower pentacene layer plays a role in charge carrier transport through the VOFET. To test this, one may vary the source insulator material and deposition process so as to find a less harmful material system and then investigate how the use of this system affects the VOFET performance. This will be done in the remainder of this section.

	V_{th} [V]	g_m [µS]	S [V/dec]	On/Off ratio	μ [cm^2/Vs]
w/o oxide	-0.70	0.99	0.67	1.5 x 10^4	0.20
w/ oxide	-0.88	0.46	0.90	2.6 x 10^3	0.07

Table 5.1.: Parameters extracted from the transfer curves displayed in figure 5.2.

[2]For such lift-off results the wave-like topography has been observed to change during imaging with a microscope. The way in which these changes occur suggests that residuals of HFE still present on the sample diffuse in and out of the gaps between the Au contact and the underlying pentacene.

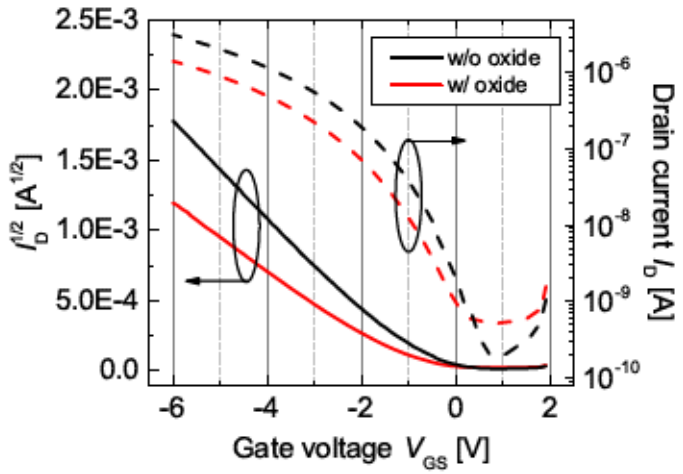


Figure 5.2.: Transfer characteristics of an OFET consisting of 25 nm pentacene, 50 nm Au and a sputtered layer of 120 nm SiO_2 on the standard Si substrate with 30 nm of Al_2O_3. A reference device without the sputtered SiO_2 layer is shown in black. The applied drain-source voltage is V_{DS} = -6 V.

5.1.1. OXIDE SOURCE INSULATORS

Presumably, the damage of the pentacene layer during sputtering is caused mostly by the impact of high-energy ions on the pentacene surface. As this surface is very rough due to the polycrystalline growth of pentacene, it must be assumed that some of these damaged impact sites are located very close to the substrate surface and thus close to or even inside the conductive channel of OFETs, which explains the reduced field-effect mobility determined in the OFET measurements. If this is indeed the case, the use of thicker pentacene layers or a sputtering process with reduced ion energy will improve the measured field-effect mobility. To test this hypothesis, a set of lithographically patterned OFETs is fabricated with varying thicknesses of the active pentacene layer. As before, a 100 nm-thick layer of SiO_2 is sputtered on top of the OFET prior to lift-off in HFE at a constant plasma source power of 90 W. In a second set, the pentacene layer thickness is kept constant at 20 nm and the plasma source power during SiO_2 sputtering is varied instead. The field-effect mobilities extracted from these OFETs are shown in figure 5.3.

It is obvious from these data that an increase in pentacene layer thickness does indeed reduce the risk of damaging those parts of the film which constitute the transistor channel. The variation in plasma source power also shows the expected trend: A higher sputtering power leads to increased damage to the pentacene. Unfortunately, it was also found that when significantly reducing the sputtering power, the insulating quality of the resultant

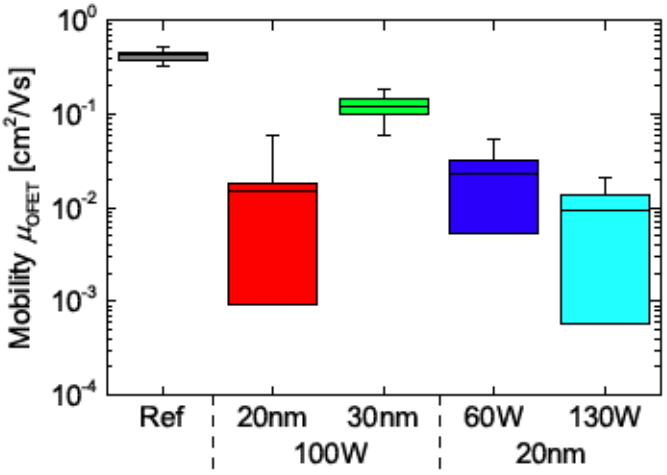


Figure 5.3.: Field-effect mobilities of a series of lithographically patterned pentacene OFETs with Au contacts and dimensions of $L = 50\,\mu m$ and $W = 2500\,\mu m$. A layer of 100 nm SiO_2 is sputtered on top of the OFETs depicted in red, green, blue and cyan prior to the lift-off in HFE, while the grey box indicates a standard OFET sample with the same dimensions. The box area indicates the interval of 25% to 75% of the mobility distribution, while the whiskers indicate the interval of 1.5 standard deviations.

SiO_2 is also reduced (data not shown here). A source power of 100 W therefore seems a good compromise, especially since the larger effect seems to be produced by a variation in pentacene layer thickness anyway.

While these results prove that it is possible to adjust the processing parameters for the pentacene layer and sputtering process in order to reduce the damaging effect to the pentacene, it is also worth to examine alternative insulating materials and deposition techniques. One such alternative deposition technique might be the thermal deposition of SiO_2 from a crucible, as done for other materials in this thesis (see chapter 4). This, however, is not a trivial matter: The optical transparency and high sublimation point of SiO_2 require special evaporators suitable for high-power processes. One such source is available from Kurt J. Lesker company and was tested at IAPP for precisely this purpose. This source, however, was unable to produce satisfying results[3] and SiO_2 deposition by electron beam (e-beam) evaporation was equally unsuccessful[4], necessitating a search for alternative insulating materials.

One such alternative is the common high-k dielectric Al_2O_3, which is already employed in the VOFET geometry as the gate dielectric. This material is typically deposited by atomic

[3]The crucible inside the evaporator melted during the course of these tests.
[4]The e-beam unit available in UFO II reached deposition rates of only 0.05 Å/s and the other e-beam sources available at IAPP produce porous layers with inferior insulating properties.

layer deposition (ALD) with substrate temperatures of approximately 250°C. While such processing conditions are unsuitable for the deposition of Al_2O_3 on top of the VOFET source contacts, the ALD system available at IAPP (see chapter 4) also includes a plasma source with which it is more easily possible to drive so-called plasma-enhanced ALD (PE-ALD) processes at processing temperatures of ≤100°C. The manufacturer of the system claims that the geometry of the process chamber prevents direct contact between the plasma-generated UV radiation and the substrate, so that oxide deposition on top of organic layers should be possible. However, as demonstrated by Michael Sawatzki in his master thesis [275], some damage to the pentacene layer in OFETs still occurs when Al_2O_3 is deposited on top of these OFETs by PE-ALD at a substrate temperature of 100°C (see figure 5.4).

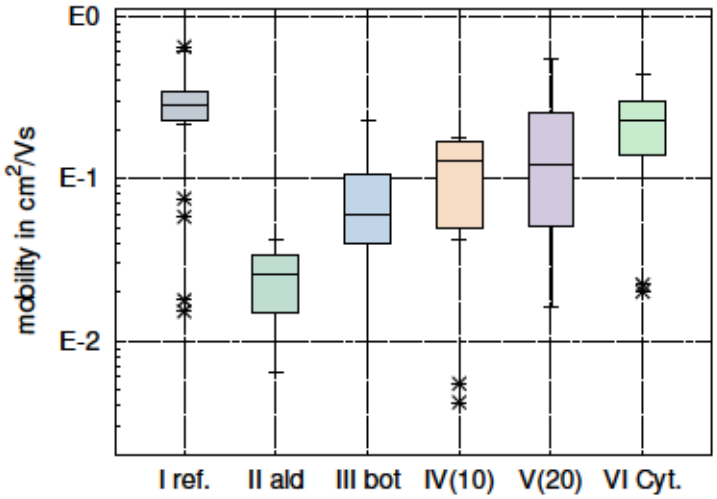


Figure 5.4.: Field-effect mobility distribution for a set of 25 devices per OFET sample. Box areas represent the interval from 25% to 75% of the data range and whiskers contain 1.5 standard deviations. Outliers are indicated as points. Samples are denoted as follows:
I ref.: reference sample without any insulator on top of the contacts
II ald: 35 nm of Al_2O_3 on top of the contacts
III bot: pentacene layer thickness increased to 50 nm, otherwise identical to II
IV(10): like II, but with 10 nm of pentacene between the contacts and the oxide as protection layer
V(20): like II, but with 20 nm of pentacene between the contacts and the oxide as protection layer
VI Cyt.: like II, but with 50 nm of pentacene between the contacts and the oxide as protection layer.
Figure taken from ref. [275].

Michael Sawatzki was further able to show that the non-directional deposition of Al_2O_3 during ALD results in coverage of the vertical undercut in underlying photolithographic

masks, thus hindering efficient lift-off of such masks. Indeed, when depositing layers of more than 30 nm Al_2O_3 by ALD, a lift-off is no longer possible, meaning that only thin layers of ALD-deposited Al_2O_3 can be structured by the photolithography technique used in this thesis. As the ability to be structured by photolithography is an essential requirement for any source insulator in the VOFET geometry[5], this imposes a limit to the applicability of Al_2O_3. While the source-drain leakage currents measured in VOFETs with 30 nm Al_2O_3 as the source insulator were comparable to those measured for the conventional 100 nm of sputtered SiO_2, such thin insulating layers in the source-drain overlap region are not desirable, as they increase the parasitic overlap capacitance of these two contacts and may thus hinder high-frequency operation of the VOFET.

Other metal oxides may either prove to be insufficient insulators (this was found to be the case e.g. for thermally deposited MoO_3, which was also tested as a potential SiO_2 replacement) or come with processing issues similar to those of SiO_2 and Al_2O_3(which is the case for any sputtered or ALD-deposited oxide).

5.1.2. ORGANIC SOURCE INSULATORS

Previous efforts in manufacturing OFETs on flexible substrates have demonstrated the good performance of polymer insulators as gate dielectrics with low processing temperatures. Polymer insulators such as CYTOP [100] or PVA [276] therefore seem viable alternatives to using metal oxides as source insulators in VOFETs. Here, too, the need to structure the source insulator on top of the source and organic semiconductor imposes a limit to the applicability of many materials. Ideal candidates are therefore photoresist materials, which can be structured directly on top of the source contact through an additional photolithography step [213, 214], and such insulators which can be evaporated through the same photolithography mask as the source contacts.

The two polymeric resists which are used for photolithography within this thesis both appear to be suitable insulator candidates at first glance. The use of ma-P1210, however, while providing the option to reduce the resist thickness to the order of 100 nm through suitable dilution[6], again necessitates the use of a protective layer to prevent damage of

[5] Structuring the source insulator by deposition through a shadow mask has been considered previously, but this results in a very large overlap of the insulator into the vertical channel and thus prevents transistor operation. Etching processes are equally problematic due to the potential damage to the organic semiconductor.

[6] This has been tested by Dipl.-Phys. Eric Jehnes in the course of his work at IAPP.

the organic semiconductor. Consequently, it should be ruled out as a good and easy-to-use option for the VOFET geometry. Orthogonal Inc., the supplier of Ortho 310, also provides a light-sensitive polymer similar to Ortho 310, which may be used as a negative photoresist. This resist, OSCoR 4000, can be diluted in its stripper (stripper 700, *Orthogonal Inc.*) and spin-coated to produce different layer thicknesses. To test its insulating properties, m-i-m devices with varying OSCoR layer thicknesses and Al contacts were prepared and their *jV* characteristics measured. The results are shown in figure 5.5 together with those obtained from a similar m-i-m structure with 100 nm SiO_2 as the insulator.

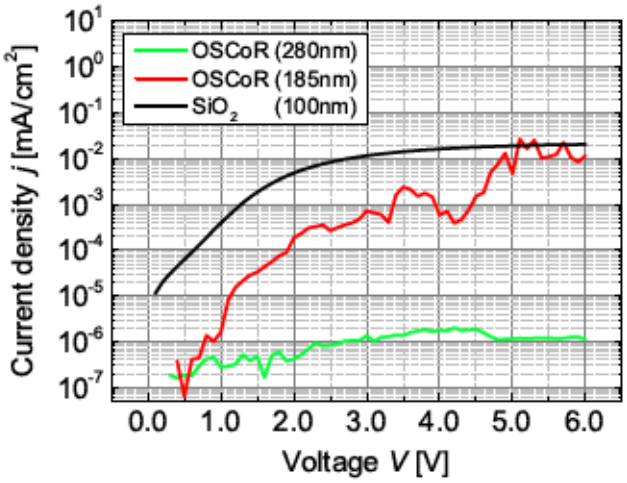


Figure 5.5.: *jV* characteristics of m-i-m structures with Al contacts and Ortho 310 in different thicknesses. A reference device with SiO_2 as the insulator is also shown.

While 200 nm of OSCoR (obtained through spin-coating a 1:3 solution of OSCoR and stripper 700 at 3000 rpm for 30 s) evidently do not provide sufficient electrical insulation to outperform SiO_2, OSCoR diluted in a 1:2 weight ratio with stripper 700 and spin-coated at 3000 rpm for 30 s gives a layer thickness of 300 nm and produces leakage currents of only 20 µA/m^2, thus outperforming SiO_2 by four orders of magnitude. While it was verified that such thin OSCoR layers can still be structured in a standard photolithography and lift-off process, their use as VOFET source insulators requires precise alignment of the respective lithography pattern with the underlying source contact. For the maskless exposure system used in this thesis (see chapter 4), such precise alignment could not be achieved. However, it was later shown by Michael Sawatzki that OSCoR is indeed a well-functioning alternative to SiO_2 when structured with a high-resolution mask aligner (see the master thesis of Michael Sawatzki for details [275]).

Organic insulators which can be deposited by the conventional thermal evaporation method are hard to come by. While e.g. polyethylene has been reported to be deposited this way on top of an already existing Al_2O_3 layer [277], reports of a stand-alone polymer dielectric which can be evaporated are difficult to find. In 2008 however, Jung *et al.* reported on a thermally deposited, hydrophobic small molecule organic insulator which was used to encapsulate pentacene OFETs and thus increase their life-time in ambient conditions [278]. Later, Kraus *et al.* successfully employed the same material, the long alkane tetratetracontane (TTC, see table 4.3), as a substrate passivation layer for OFETs [85]. In 2012, Göllner *et al.* demonstrated a double-gated pentacene OFET using TTC as the dielectric for the electrolyte top gate, thus demonstrating the potential of TTC as an organic insulator [279].

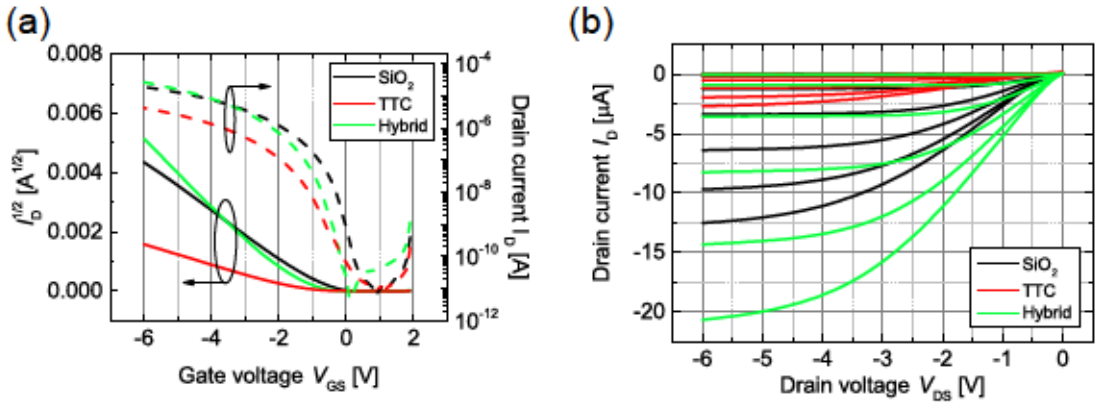


Figure 5.6.: Transfer characteristics (a) and output characteristics (b) of VOFETs with source insulators made of 100 nm SiO_2 (black), 100 nm TTC (red) and a combination of 25 nm SiO_2 and 75 nm TTC (green). The applied drain voltage for the transfer characteristics is V_{DS} = -6 V. The gate voltage for the output characteristics was varied from 0 V to -6 V in steps of 1 V.

	V_{th} [V]	g_m [µS]	S [V/dec]	On/Off ratio
SiO_2 insulator	-0.70	5.77	0.31	3.0×10^6
TTC insulator	-1.48	1.44	0.51	1.0×10^6
Hybrid insulator	-1.40	9.35	0.26	6.1×10^6

Table 5.2.: Performance parameters extracted from the transfer curves displayed in figure 5.6 (a).

Figure 5.6 shows the transfer and output characteristics of pentacene VOFETs in which different source insulators are employed: 100 nm SiO_2 as the reference device (shown in black), 25 nm SiO_2 with 75 nm TTC on top as an organic-inorganic hybrid insulator (green) and 100 nm pure TTC as a stand-alone organic insulator (red). The extracted

performance parameters are given in table 5.2. Evidently, the sample containing the hybrid insulator outperforms the pure organic and inorganic source insulators in every respect but the threshold voltage. The higher transconductance and On/Off ratio indicate that the pentacene layer underneath the source electrode is less damaged when depositing a thinner SiO_2 layer, while the hybrid insulator still provides sufficiently good insulating properties to keep the source-drain leakage currents low. The increase of V_{th} with introduction of a TTC layer into the VOFET geometry may be attributed to the manufacturing process: As suggested by Kraus *et al.* for TTC on SiO_2 [85, 88], the VOFET samples containing TTC layers were annealed in a nitrogen glovebox for two hours at 60 °C after TTC deposition. According to Kraus *et al.*, this leads to a reorganisation of the TTC from the initial cluster growth into a closed film with clearly defined terraces of 5 nm height difference (the length of one TTC molecule along its long axis). Clearly, this annealing step also leads to a diffusion of TTC over the edge of the VOFET source contacts, thus providing a considerable insulator overlap. If charge carriers are injected primarily from the bottom surface of the source contacts, as expected, then such an increased insulator overlap naturally requires a higher VOFET threshold voltage.

For the case of VOFETs using only TTC as the source insulator, only a single working device was found on a sample containing approximately 30 VOFETs, all other devices showed source-drain short-circuits. Repetitions of this experiment yielded no working devices with TTC insulators at all. The reason for this poor yield becomes apparent when considering the growth mode of TTC. Figure 5.7 shows an AFM image of the terrace-like morphology of annealed TTC stacking vertically on SiO_2, as reported also by Kraus *et al.* [88]. Here, the darkest regions, according to the height scale bar shown on the right, correspond to one or two monolayers of TTC, while terraces are formed primarily in the third monolayer and point-like features are caused by a fourth monolayer.

This formation of closed films with neatly stacked TTC molecules seems possible only on SiO_2. Similar experiments with TTC evaporated on top of different materials (glass substrates, metals, metal oxides and organic semiconductors[7]) and combined with various annealing procedures yielded always the same result: Surfaces other than SiO_2 cause the formation of high TTC needles, which cannot be flattened by annealing. This was found also by Nakayama *et al.* for TTC grown on rubrene single crystals [280] and by the group

[7]Materials tested on top of Si substrates with 30 nm Al_2O_3: 30 nm of Al, Au, Cr, SiO, pentacene and C_{60}. The growth of TTC directly on the Al_2O_3-covered substrate was also investigated.

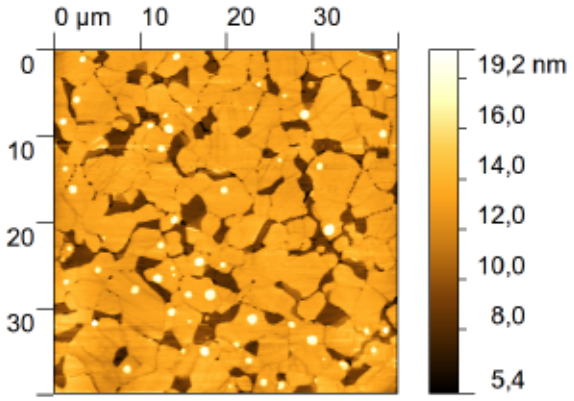


Figure 5.7.: Tapping mode AFM image of nominally 20 nm TTC on an Si wafer with 200 nm thermally grown SiO_2. The sample was annealed in a nitrogen glovebox for two hours at 60 °C prior to imaging.

of Prof. Wolfgang Brütting (Universität Augsburg, Germany) for various other materials according to a discussion with Prof. Brütting in 2013. For the case of nominal TTC layer thicknesses $\geq$ 50 nm, the height of these TTC needles may even exceed 1 µm and while closed layers of TTC may be formed underneath these needles, they are evidently not sufficiently insulating to prevent source-drain short-circuits in the VOFET architecture, as demonstrated by the poor yield for 100 nm TTC as the sole source insulator. The reasons for TTC's peculiar behaviour on SiO_2 are currently unclear and a more thorough investigation is certainly required in order to clarify this matter. This, however, was omitted here so as not to digress too far from the main topic of this work. Suffice it to say that TTC may prove to be an interesting insulator in the future if its growth can be controlled. The hybrid insulator however, when considering the increased processing effort, does not show sufficient improvement in performance and reproducibility to make it truly superior to the 100 nm SiO_2 insulator. This "standard" SiO_2 insulator will therefore be used for the remainder of this work so as to provide a consistent reference.

5.2. EFFECTS OF THE PENTACENE MORPHOLOGY

As demonstrated in the previous section, the choice of the source insulator may have an effect on the VOFET performance in terms of transconductance and On/Off ratio. This effect, however, seems to be related mostly to the insulator's influence on the semiconductor layer underneath the source electrodes. Consequently, a more direct method of improving device performance may be to improve the quality of this semiconductor layer.

Thermally evaporated pentacene is already a good material choice as it is easy to process and provides good transport properties in many conventional OFET geometries. In general, this holds true also for the VOFET architecture. In this case, however, the morphology of pentacene proves to be a certain drawback. As reported by Kleemann *et al.* for the case of C_{60} OFETs structured by photolithography, residuals of the protective resist Ortho 310 may remain on the semiconductor surface after the pattern transfer step (step 3 in figure 4.3) and thus increase contact resistance in lithographically patterned OFETs [90]. This effect increases with increasing semiconductor surface roughness and is thus more pronounced for polycrystalline pentacene films than for the amorphous C_{60}. It is also present in the VOFET architecture and may here be combined with an increased channel resistance due to resist residuals in the vertical channel region between the lower and upper semiconductor layer (see figure 5.8).

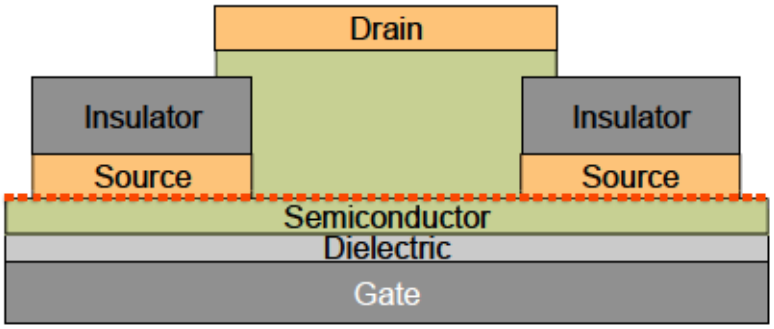


Figure 5.8.: Schematic representation of a VOFET structure with the position of Ortho 310 residuals marked as a dotted orange line.

As Cosseddu *et al.* have shown, the average grain size and surface roughness of polycrystalline pentacene films may be controlled by the deposition rate for evaporated films, while the crystallinity remains unchanged [160]. This is shown also in figure 5.9 (a) to (c) for pentacene films evaporated onto Si wafers with 20 nm Al_2O_3 at deposition rates of 0.5, 1.5 and 2.5 Å/s (see appendix A for XRD spectra). Figure 5.9 (d) to (f) further shows that also the nominal thickness of the pentacene film has an influence on grain size and surface roughness, since the growth regime eventually changes from the thin film phase (broad, flat crystallites, visible in all parts of figure 5.9) to the onset of a bulk phase (rod-like grains, visible particularly in figure 5.9 (f)). This trend, too, can be confirmed by XRD (see appendix A).

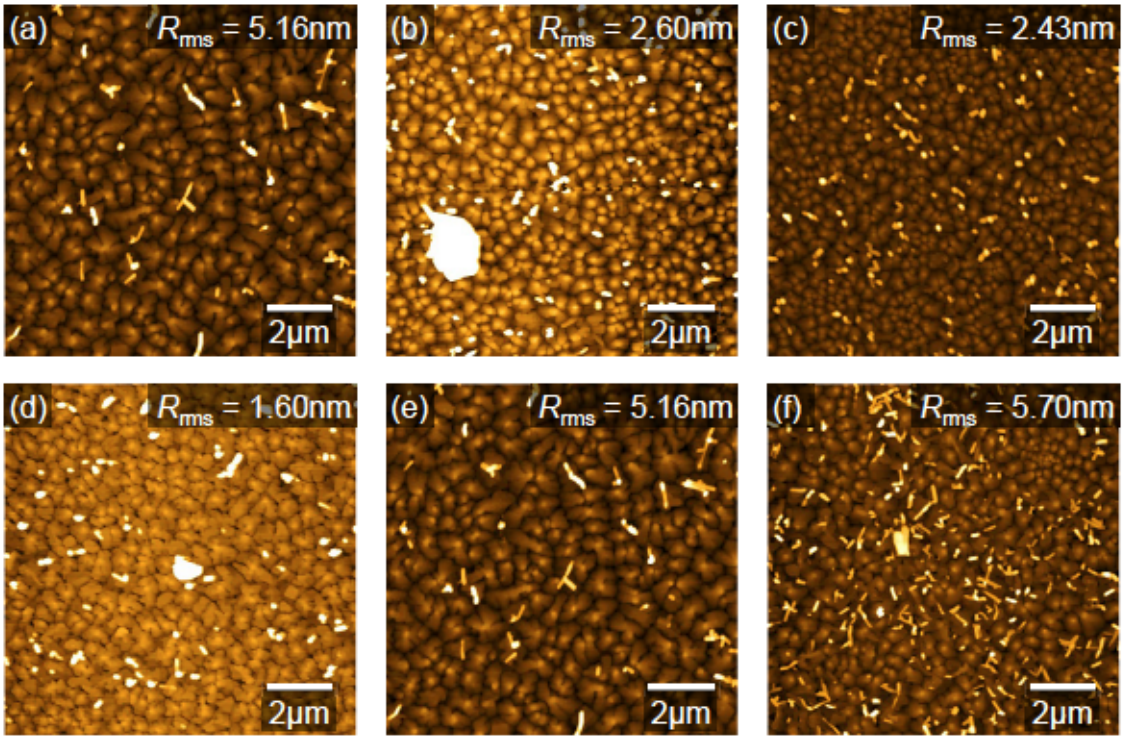


Figure 5.9.: Tapping mode AFM images of pentacene evaporated onto Si wafers with 30 nm ALD-deposited Al_2O_3 on top. (a) to (c): Layer thickness of 20 nm with deposition rates of 0.5 Å/s, 1.5 Å/s and 2.5 Å/s. (d) to (f): Deposition rate of 0.5 Å/s with layer thicknesses of 10 nm, 20 nm and 30 nm.

When such pentacene films of varying surface roughness are used as the bottom semiconductor layers in VOFETs, a dependence of the transfer and output characteristics on deposition rate is observed, where the strongest effects are noticeable in the output characteristics (see figure 5.10). In particular, the output characteristics at small V_{DS} become distinctly non-linear for pentacene films with higher deposition rates, a feature which is suggestive of contact limitation (see chapter 2). Additionally, one observes a decrease in transconductance with increasing deposition rate.

	V_{th} [V]	g_m [µS]	S [V/dec]	On/Off ratio
0.5 Å/s	-0.80	12.15	0.41	6.3×10^5
1.5 Å/s	-0.50	9.52	0.79	4.4×10^5
2.5 Å/s	-0.70	5.68	0.28	1.9×10^6

Table 5.3.: Performance parameters extracted from the transistors displayed in figure 5.10.

The occurrence of contact effects naturally leads to the conclusion that either the contact resistance increases for pentacene films deposited at a higher rate or the channel resistance must decrease. The former is considered as unlikely since the higher deposition

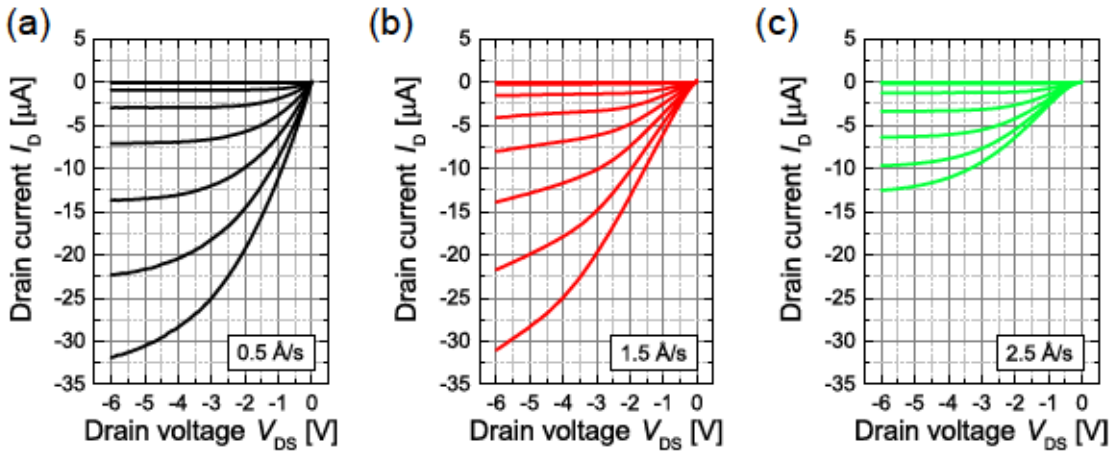


Figure 5.10.: Output characteristics of pentacene VOFETs with the bottom pentacene layer evaporated at different deposition rates. The gate voltage was varied in steps of 1 V, with the maximum gate voltage set to V_{GS} = -6 V.

rate causes smoother films and should therefore yield a better - rather than worse - contact between the Au electrodes and the underlying pentacene. To verify this, a series of OFETs with Au contacts and pentacene evaporated at the same rates was also investigated and a TLM analysis was performed. The extracted contact resistance, however, shows no clear dependence on the deposition rate (see figure 5.11 (b)). This indicates that at least the pattern transfer with HFE solvents can be performed without leaving vast quantities of resist residuals, although the initial data of Kleemann *et al.* suggested otherwise [90]. On

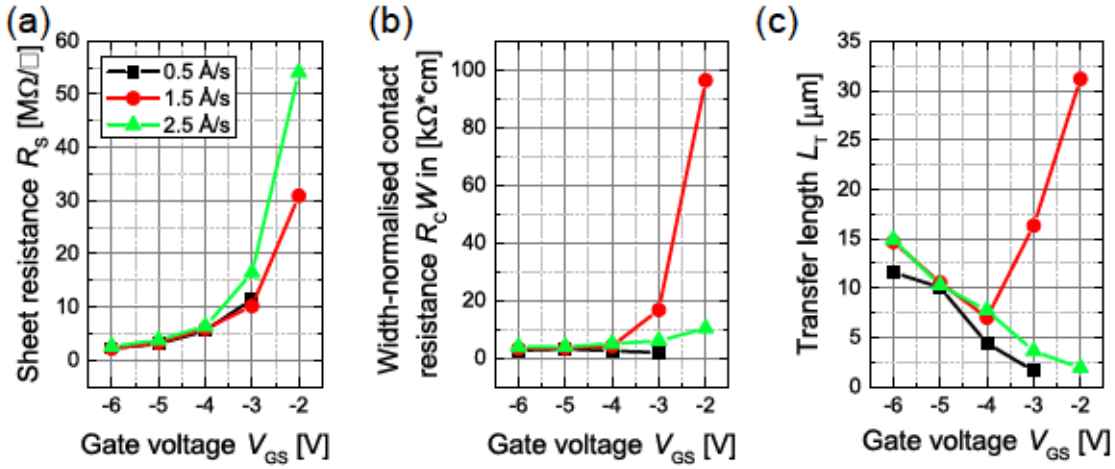


Figure 5.11.: Sheet resistance (a), width-normalised contact resistance (b) and transfer length (c) extracted from a set of OFETs with 25 nm of pentacene deposited at different rates and 40 nm Au contacts.

the other hand, the sheet resistance data extracted in the same TLM analysis suggests that also the channel resistance in the VOFET should increase with increasing deposition

rate. This, according to Cosseddu *et al.*, would be due to a decrease in charge carrier mobility with decreasing grain size, i.e. with increasing deposition rate. Evidently, there is a contradiction between the increasing channel resistance due to a lowered mobility and the occurrence of contact effects observed in the VOFET characteristics in figure 5.10. This apparent paradox may be solved thus: While the mobility in the lower pentacene layer may decrease with increasing deposition rate, the surface of this layer becomes smoother. If one assumes that the lift-off process in HFE (see chapter 4) is less efficient in removing Ortho 310 residuals than the pattern transfer process[8], it is likely that the channel resistance is indeed affected by resist residuals and thus by semiconductor surface roughness. Then, the observed output characteristics are the result of a convolution of increasing channel resistance due to decreasing mobility and decreasing channel resistance due to fewer resist residuals.

Two important conclusions may be drawn from these observations: For one, the VOFET performance appears to depend significantly on the quality of the photolithography process, more precisely the extent to which the resist layers can be removed from the semiconductor surface. Secondly, the data presented in this section suggest that charge carrier transport underneath the source electrode, i.e. in the bottom semiconductor layer, is not negligible in this vertical transistor architecture.

5.3. SUMMARY

By simple variations of the processing conditions and materials used in the VOFET architecture, it has been possible to identify several parameters which have an effect on the overall VOFET performance. The source insulator, made hitherto of 100 nm SiO_2 and deposited by magnetron sputtering, determines not only the amount of source-drain leakage current, but the manner in which it is deposited may also affect the quality of the organic semiconductor underneath and the success of the lift-off process. Among the possible alternatives suggested here, patterned fluoro-resist layers or thermally deposited organic insulators appear to be the most promising choices, provided their deposition and structuring can be controlled sufficiently in the future. For the purpose of this work, however, the state-of-the-art SiO_2 insulator must suffice in order to ensure reproducible

[8] This is easily possible as the pattern transfer process includes a combination of puddle-etching and spin-rinsing with HFE, while the lift-off is performed simply by dipping the sample into HFE.

results and easy processing. In this case, good control over the pattern transfer process is vital, as this not only appears to control the amount of SiO_2 overlapping from the Au contact edge into the vertical channel region, but a good pattern transfer procedure also seems to avoid an increased contact resistance due to resist residuals underneath the Au contacts.

It was possible to show that this latter effect, as well as the channel resistance, can also be partially controlled by the rate at which the bottom semiconductor layer is deposited. It was further observed that this bottom semiconductor layer may also play a significant role not only in charge carrier injection, but also in charge carrier transport. As the VOFET is intended as a short-channel device governed mostly, if not entirely, by transport through the vertical channel, it is evidently necessary to determine the extend to which this bottom semiconductor layer plays a role in the charge transport. The general question of charge carrier transport in this vertical architecture will therefore be dealt with in more detail in the following chapter.

6. CHARGE TRANSPORT IN THE VOFET

This chapter will focus on the operational principle of the VOFET geometry. In particular, it will discuss a 3D simulation of the VOFET geometry created and performed by Dr. Klaus Gärtner, Dr. Annegret Glitzky, Dr. Thomas Koprucki and Dr. Doan Duy Hai from the Weierstrass Institute for Analysis and Stochastic (WIAS) in Berlin. The aim of this simulation is to provide information on the charge carrier flow and potential distribution inside the VOFET geometry. The data produced by the WIAS simulation will be compared to experimental data and an attempt to visualise the vertical channel by light emission will be presented. These latter experiments were performed by Michael Sawatzki (IAPP) in his Master thesis. Discussion of the operational mechanism of the VOFET will further be aided by an electron microscopy study on the VOFET structure performed by Dr. Petr Formánek (IPF).

The previous chapter has clearly illustrated the experimental challenges in preparing VOFET samples and has demonstrated how different, sometimes even opposite effects can convolute to produce transistor characteristics which are not always easily understood. In particular, the presented experimental results suggest a considerable contribution of lateral transport underneath the source electrode to the overall transistor characteristics, which may be due to an overlap of the source insulator into the vertical channel region. It is obvious from these findings that both the exact geometry and the charge carrier flow through this geometry need to be understood in more detail. As certain charge transport effects may not be visible or at least easily identifiable in the real device due to the experimental limitations detailed previously, a combination of experimental investigations and numerical simulations must be used in order to understand the charge transport processes in the VOFET in more detail.

This chapter will therefore begin by discussing the exact geometry and layer arrangement of the VOFET based on electron microscopy investigations of VOFET samples. This structural information will then be used to set up a numerical simulation of the working VOFET which yields first results concerning the ideal behaviour of the VOFET. The results produced by the simulation are checked against experimental data. Namely, the formation of the vertical channel is analysed in more detail using both the simulation data and experimental results provided by Michael Sawatzki in his master thesis [275]. Lastly, by using the peculiar charge transport properties of pentacene, predictions made by the simulation with regards to layer thickness and mobility variations will be tested and conclusions will be drawn regarding the ideal VOFET.

6.1. SIMULATING CURRENT FLOW IN THE VOFET

In order to gain an understanding of the fundamental working principles of the VOFET and of its behaviour under ideal conditions, a numerical simulation of charge carrier transport in the known VOFET geometry is necessary. This simulation is performed by Dr. Duy Hai Doan, Dr. Thomas Koprucki, Dr. Annegret Glitzki and Dr. Klaus Gärtner from the Weierstrass Institute for Applied Analysis and Stochastic (WIAS) in Berlin. For this simulation to produce accurate results which are qualitatively and quantitatively comparable to the experimental data obtained from real devices, the layer arrangement and geometry of the real VOFET

need to be investigated. As chapter 5 has demonstrated, the hitherto assumed structure of a VOFET stack with well-aligned vertical layer edges (as shown in figure 5.8) appears to be incorrect.

6.1.1. DETERMINING THE REAL STRUCTURE OF THE VOFET

The precise structure of the VOFET is best examined using electron microscopy, which provides a high resolution for measuring not only the surface topology of a VOFET sample, but to image also the vertical stacking of the individual layers, with a contrast sufficient to distinguish organic, metallic and oxide layers. The vertical layer arrangement is examined by cutting a lamella of the VOFET structure (see chapter 4) and scanning it with transmission electron microscopy (TEM), while the VOFET sample surface is investigated using scanning electron microscopy (SEM). Both measurements are performed by Dr. Petr Formánek from IPF. Figure 6.1 shows a top view of the overlap area between the source and drain electrodes of the VOFET, as obtained by SEM. The source and drain areas are marked in blue and orange. The image also shows a clear horizontal line feature. Its distance to the source edge (approximately 3.2 µm) is marked with a red line. Comparing the

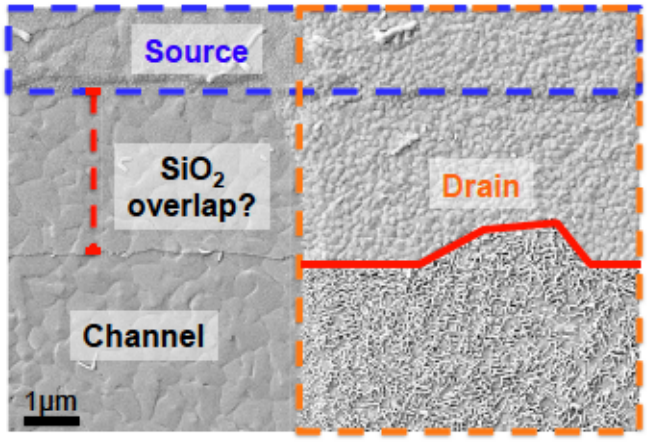


Figure 6.1.: SEM top view of the source-drain overlap region in the VOFET. The source area is indicated in blue, the drain is marked as orange. The dashed red line indicates the proposed length of the source insulator overlap and the solid red line indicates the edge of the vertical channel region. Reproduced from ref. [268].

growth regimes of pentacene in the different regions, one observes that a dominant bulk phase, i.e. rod-like crystallites, is only visible in the bottom right corner of this image. Consequently, the top layer of pentacene, which is evaporated through the same mask as the drain electrode, grows directly on top of the lower pentacene layer only in this one

region. Where the source and drain overlap, the second pentacene layer forms a thin film phase on the surface of the source insulator. As there is little difference between the pentacene morphology in the source-drain overlap region (top right corner of the image) and the part directly underneath up to the horizontal line feature, it must be concluded that the second pentacene layer grows on top of SiO_2 also in this region, meaning that the horizontal line feature must mark the edge of SiO_2 overlapping the edge of the source contact. The structure of the VOFET would then more precisely be described by the schematic shown in figure 6.2 (b) (as compared to the previous version, shown in figure 6.2 (a)).

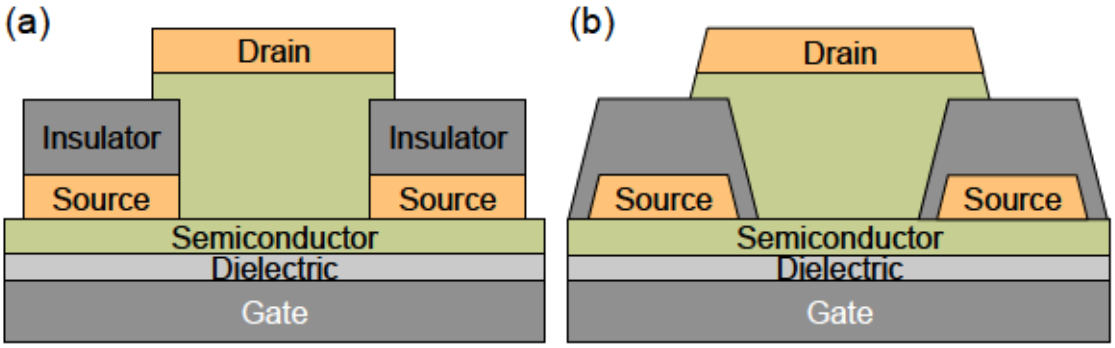


Figure 6.2.: Schematic representation of the VOFET stack: (a) Simplified picture without insulator overlap as used so far, (b) modified schematic including a small source insulator overlap.

The existence of a source insulator overlap can be verified by TEM measurements on lamella cuts (produced by focused ion beam, FIB) of different regions of the VOFET. Figure 6.3 shows such images of the vertical layer arrangement of the VOFET for the centre of the source-drain overlap region (figure 6.3 (a)), the edge of this overlap region (figure 6.3 (b)) and the vicinity of the horizontal line feature observed in the SEM image (figure 6.3 (c)). The contrast and thickness of the different layers in the TEM image allows to identify them precisely, as marked in figure 6.3. It is obvious from this data that the thick SiO_2 layer used as the source insulator does indeed overlap the source edge by a noticeable amount and that its vertical "edge" is in fact a thinning tail, as is also the case for the source electrode.

It follows that the lower pentacene layer has indeed an increased chance of getting damaged by fast ion impact during the sputtering process if SiO_2 is deposited directly onto the pentacene surface in the vicinity of the source contact. Furthermore, the existence of this insulator overlap and its thickness at the source edge suggest that charge carrier injection must take place only from the bottom surface of the source contact. In this case,

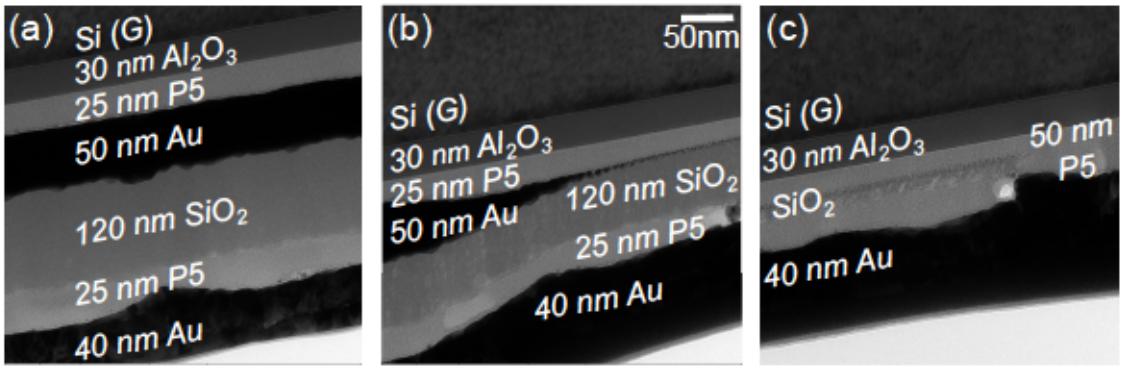


Figure 6.3.: TEM images of lamella cuts through the VOFET in three different regions: (a) the centre of the source-drain overlap region, (b) the edge of the source-drain overlap region and (c) the approximate position of the SiO_2 edge observed in figure 6.1. Individual layers are labelled and the stack is shown in reverse, i.e. with the Si substrate on top and the Au drain electrode on the bottom.

charge carriers may accumulate at the gate dielectric interface or at the bottom surface of the source insulator before moving into the vertical channel. It seems reasonable to assume that they diffuse along one of these interfaces until they have passed the source insulator overlap edge and only then begin to drift upwards into the vertical channel due to the applied source-drain field.

6.1.2. THE NUMERICAL SIMULATION

The numerical simulation performed by the team at WIAS uses the Oskar3 solver (created by Dr. Klaus Gärtner, WIAS) to find solutions to the classical van Roosbroeck equation system in a non-degenerate semiconductor with a self-consistent electric field [281]:

$$\begin{aligned} -\nabla\vec{r}\cdot\varepsilon_0\varepsilon_r\nabla_{\vec{r}}\Phi &= e(c-n+p) \\ \frac{\partial n}{\partial t} - \nabla_{\vec{r}}(D_n n_i \nabla_{\vec{r}}\frac{n}{n_i} - \mu_n n\Phi) + R(n,p) &= 0 \\ \frac{\partial p}{\partial t} - \nabla_{\vec{r}}(D_p n_i \nabla_{\vec{r}}\frac{p}{n_i} - \mu_p p\Phi) + R(n,p) &= 0 \end{aligned} \tag{6.1}$$

Here, c is the local doping concentration, Φ the electrostatic potential and R a function representing generation and recombination processes[1]. n and p are the electron and hole densities, μ_n and μ_p are the respective carrier mobilities and D_n and D_p the diffusion coefficients associated with these carriers. For a non-degenerate system, these are given

[1] Currently, Shockley-Reed-Hall recombination (SRH) and Auger recombination processes are implemented in Oskar3.

by the Einstein relation as $D_{n,p} = \frac{k_B T}{e} \mu_{n,p}$ [30]. The respective VOFET stack is represented in a 3D simplex grid with a tetrahedral mesh, which is denser in the vicinity of important VOFET regions, such as the vertical source edge or the edge of the source insulator (see figure 6.4). The electrodes are represented as highly doped regions of the semiconductor

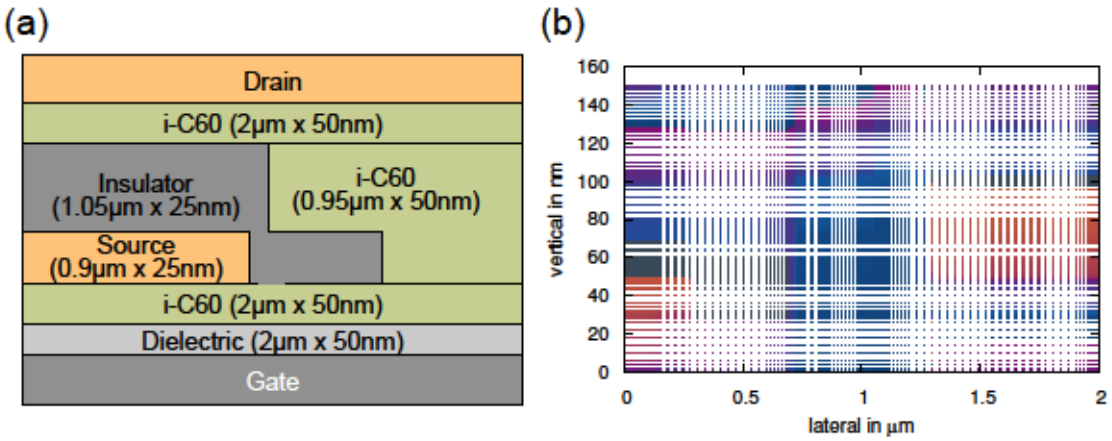


Figure 6.4.: (a) Schematic representation of the VOFET layout used for the initial simulation. The total lateral dimension of the simulation device is 2 µm. (b) 2D representation of the tetrahedral mesh grid used as data points for the numerical simulation.

(here, $n = 5\text{x}10^{21}$ cm^{-3}) with ohmic injection into the underlying intrinsic semiconductor layers and all oxide layers are treated as perfect insulators. The mobility model used to describe charge carrier transport was originally developed only for silicon and thus included the Scharfetter-Gummel approach for ionised impurity scattering, a formalism for neutral impurity scattering and Adler's model for carrier-carrier scattering, which are all combined through Matthiessen's rule [282] and modified by a velocity saturation term according to Caughey and Thomas to account for electric field dependence [283]. In more recent versions of Oskar3, the EGDM model (see section 1.2) has also been incorporated to describe more accurately the temperature- and field-dependent charge carrier transport in disordered organic semiconductors. For the purpose of VOFET simulations, however, the active material was first implemented as intrinsic, trap-free C_{60} with a constant mobility of 0.1 cm^2/Vs. To reduce the required computing power and gain a first qualitative understanding of the simulated VOFET, the lateral dimensions of the VOFET structure have also been reduced by one order of magnitude, as is visible from figure 6.4.

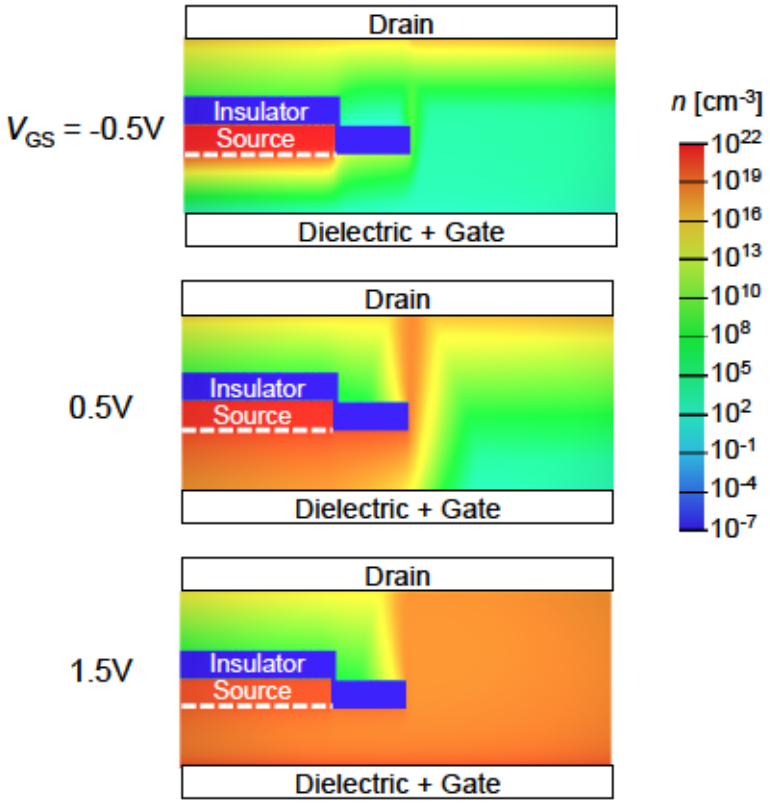


Figure 6.5.: Electron density in the simulated VOFET geometry as a function of gate bias with source and drain connected as shown in figure 6.4. The gate electrode, gate dielectric and drain electrode are shown only schematically in these images as they are of no interest for the simulation and are thus implemented only as boundary conditions. In the colour scheme used here, blue represents a low charge carrier density of 10^{-7} cm^{-3}, while red indicates high charge carrier density on the order of 10^{20} cm^{-3}. The applied source-drain voltage is V_{DS} = 1.0 V.

FORWARD BIAS

The WIAS simulation provides information on numerous variables, such as the potential distribution, charge carrier density, SRH generation rate etc. For the purpose of this work, the charge carrier density and potential distribution are of the highest interest, as they provide vital information about the functional principles of the VOFET. Figure 6.5 shows the electron density distribution inside the simulated C_{60} VOFET displayed in figure 6.4 (a) for different gate bias conditions. At negative bias, i.e. in the Off-state, charge carriers accumulate near the source contact due to the opposing gate field. A small density of electrons diffuses laterally from the source through the bulk of the semiconductor ($n \sim 10^7\,\mathrm{cm}^{-3}$) and may reach the vertical channel region if their diffusion length is sufficiently long. These charge carriers constitute an Off-state current towards the drain which is barely larger than the surrounding background density of carriers. As the gate voltage is increased beyond threshold ($V_{th} = 0\,\mathrm{V}$), more charge carriers are emitted from the source electrode and begin to accumulate in the underlying semiconductor. As in a conventional OFET, the increased charge carrier density in this region results in the formation of a conductive region. The diffusion length of carriers in this region is significantly larger, thus allowing more carriers to diffuse to the source insulator's edge and drift up towards the drain electrode. It is interesting to note, however, that for the case of a low V_{GS} in comparison to V_{DS}, the conductive accumulation region in the bottom semiconductor layer is located near the source and source insulator (compare figures 6.6 and 6.7). This is in

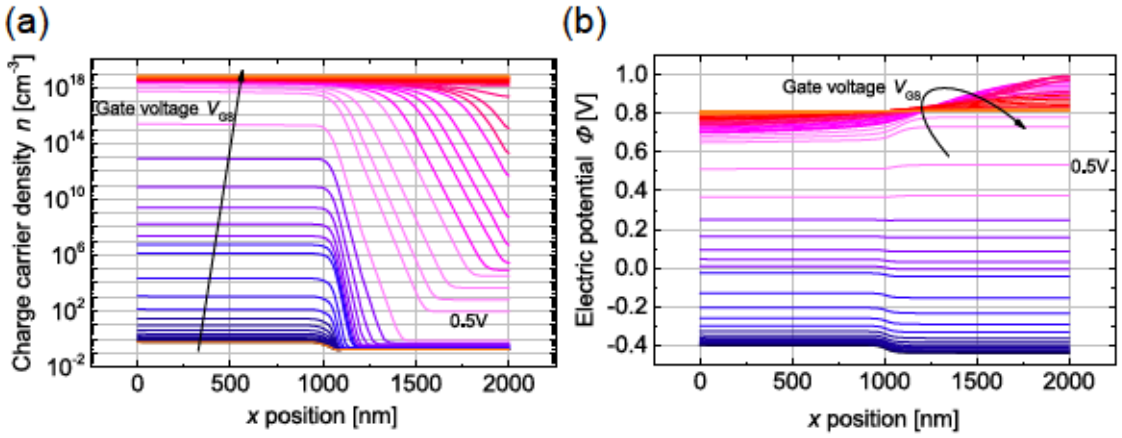


Figure 6.6.: Lateral charge carrier density (a) and electric potential (b) profiles in the bottom semiconductor layer of a VOFET with a small insulator overlap at a position y = 1 nm, i.e. 1 nm above the gate dielectric interface. Blue lines indicate low V_{GS} and red indicates high V_{GS}.

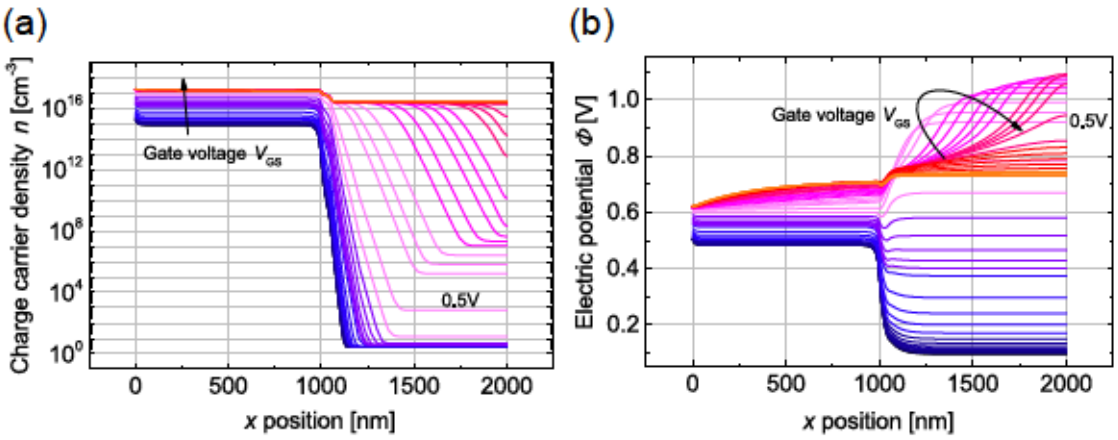


Figure 6.7.: Lateral charge carrier density (a) and electric potential (b) profiles in the bottom semiconductor layer of a VOFET with a small insulator overlap at a position y = 45 nm, i.e. 5 nm below the source contact. Blue lines indicate low V_{GS} and red indicates high V_{GS}.

stark contrast to conventional OFETs, where charge carriers always accumulate at the gate dielectric interface. In the voltage regime $|V_{DS}| > |V_{GS} - V_{th}|$, the VOFET therefore least fulfils the gradual channel approximation as the drain field here is considerably stronger than the gate field and thus leads to this shift in accumulation position. Whether or not this scenario is at all accessible in a real VOFET will depend strongly on the field distribution and thus the shape and thickness of the source insulator overlap. A comparison of the simulated geometry of a long overlap with the TEM measurements in figure 6.3, however, suggests that the drain field near the source electrode is generally much weaker in the real devices due to the overall thicker and more extended overlap. The accumulation layer may consequently be located closer to the gate dielectric interface for the saturation regime of a real VOFET.

As the gate bias is increased in the simulation, the position of the accumulation region shifts towards the gate dielectric interface and thus to a conventional OFET behaviour, where now the entire vertical channel region is gradually used to conduct carriers towards the drain. At this stage, the vertical channel is fully saturated, which manifests also as a saturation in the transfer characteristics of the simulated VOFET (see figure 6.8). From this, it can be concluded that in the ideal VOFET's linear regime, where $|V_{DS}| < |V_{GS} - V_{th}|$, the On-state current is limited by the lateral extent of the vertical channel. In the real VOFET with two source contacts (see e.g. figure 6.2), this lateral limit corresponds to the distance between the two insulator overlap edges. In real VOFETs, however, the reduced lateral

conductivity due to traps at the gate dielectric interface will prevent diffusion on this length scale, so that an exponential decrease in charge carrier density with lateral channel extent will be observed instead[2].

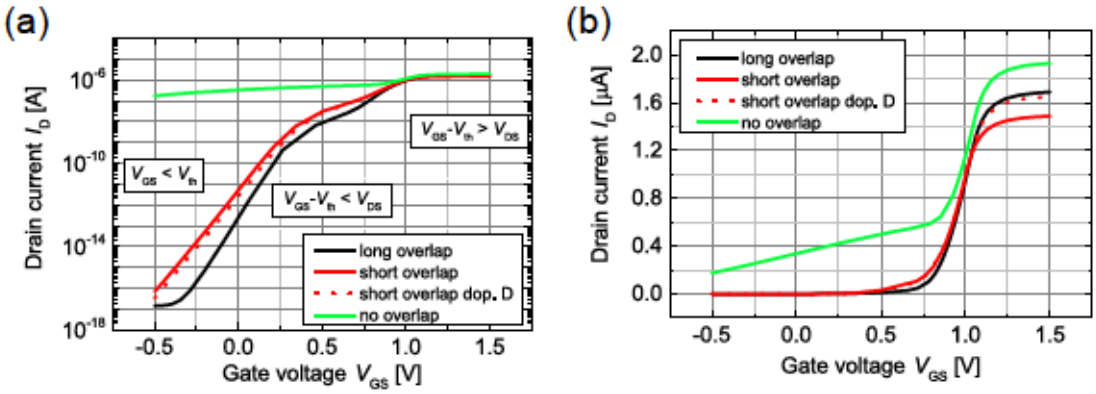


Figure 6.8.: (a) Transfer characteristics of simulated VOFETs with different device geometries: the original design with a long insulator overlap (solid black line), a considerably shorter overlap (solid red line), the short overlap with a shorter, doped drain (dotted red line) and a device without insulator overlap (solid green line). (b) The same solid curves shown once again on a linear scale. The applied source-drain voltage is 1.0 V and the corresponding charge carrier density distributions are shown in figure 6.9.

Figure 6.8 shows the transfer characteristics of several other geometries as well. The corresponding charge carrier density distributions are summarised in figure 6.9 for selected gate voltages. Here, a VOFET with an insulator overlap of only 50 nm (figure 6.9 (b) and red transfer curves in figure 6.8) as well as a device without any overlap of the insulator over the source edge (figure 6.9 (c) and green transfer curve in figure 6.8) are shown. Unsurprisingly, the lack of an insulator overlap over the vertical edge of the source contact results in charge carrier emission from that edge directly into the vertical channel. As this injection path is difficult to control with the gate field (the edge of the source being in line with the gate field rather than perpendicular to it), it produces a considerably higher Off-state current than devices with a source edge covered by the source insulator, while a long insulator overlap ensures low Off-state currents and thus a good On/Off ratio. Examining the saturation regime of the VOFET in the transfer characteristics, where $|V_{DS}| > |V_{GS} - V_{th}|$, a type of shoulder formation is found for both of the devices with an insulator overlap which has so far not been observed in experiments. By extracting lateral charge carrier density and electric potential profiles inside the vertical channel at a

[2] One might enforce the lateral saturation of the channel region by applying sufficiently high gate voltages, provided that the gate dielectric has a sufficiently high breakthrough point.

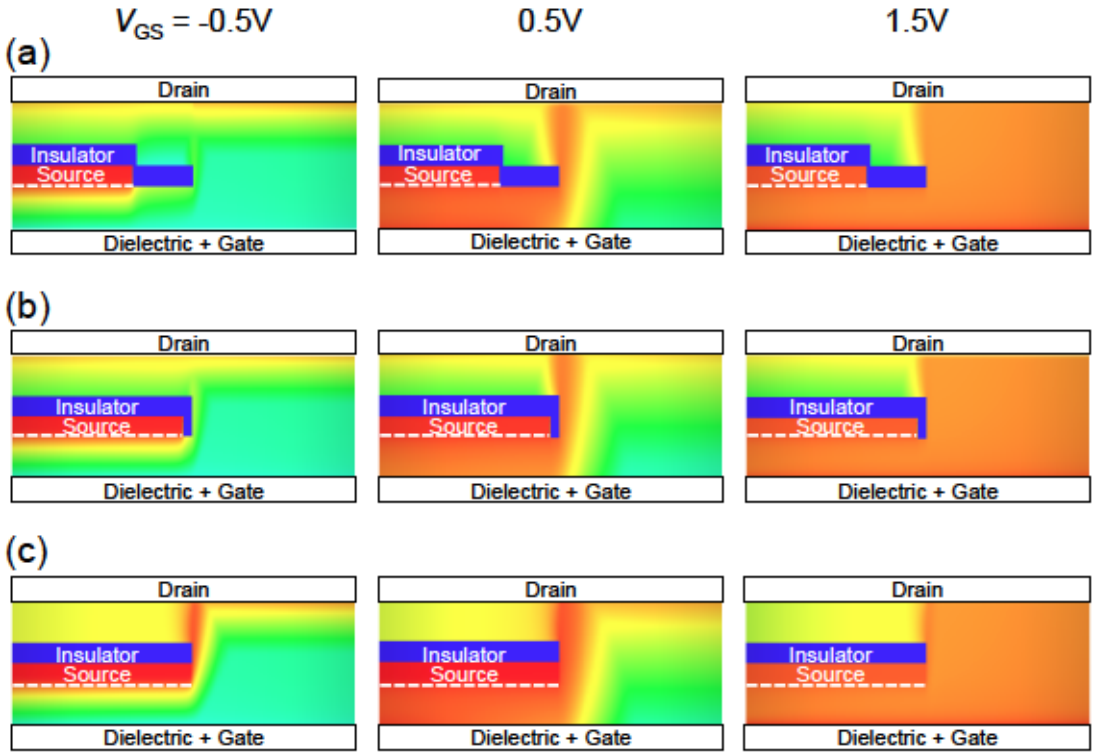


Figure 6.9.: Electron densities for simulated VOFETs with different source insulator geometries: (a) the original design with an extended insulator overlap (as shown already in figure 6.5), (b) a short insulator overlap of 50 nm and (c) no insulator overlap. The applied source-gate voltage is indicated at the top of each column of plots and the applied source-drain voltage is 1.0 V for all devices. The colour scheme is the same as in figure 6.5.

height of 90 nm from the bottom edge of the simulated area, i.e. 15 nm above the source electrode[3], one is able to observe the origins of this shoulder formation in more detail. At low V_{GS}, the charge carrier density is high in the direct vicinity of the source insulator edge, but drops rapidly with increasing lateral distance from this edge. The same holds true for the electric potential. As the gate voltage is increased gradually to 0.5 V, the carrier density rises particularly strongly at the source insulator edge and only slowly in the rest of the channel, again, this behaviour is mirrored by the electric potential, suggesting a slight shielding of the gate potential near the source edge due to the accumulation of charge carriers. Little beyond $V_{GS} = 0.5$ V, a saturation carrier density of $n = 10^{16}$cm^{-3} is reached at the edge of the source insulator. This saturation point then begins to spread through the entire vertical channel as the gate voltage is increased further towards the linear regime. At this stage, the shielding of the gate potential by charges in the accumulation layer becomes a dominant effect. It is the transition between the two regimes which produces the observed shoulder formation in the gate sweep. Evidently therefore, I_D in the regime $|V_{DS}| > |V_{GS} - V_{th}|$ depends mostly on the strength of the source-drain field, i.e. the applied V_{DS}, as well as the amount of charges injected into the vertical channel.

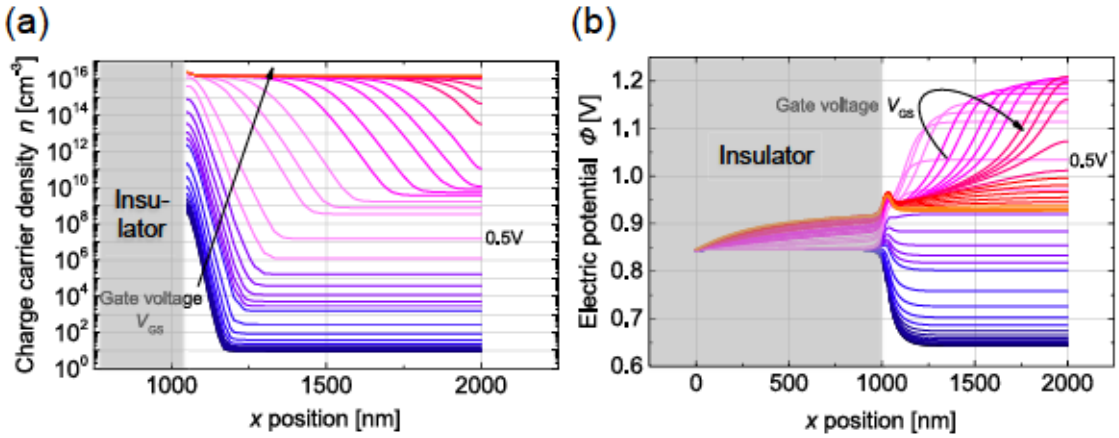


Figure 6.10.: Lateral charge carrier density (a) and electric potential (b) profiles inside the vertical channel of a VOFET with a small insulator overlap at a position y = 90 nm, i.e. 15 nm above the source contact. Blue lines indicate low V_{GS} and red indicates high V_{GS}.

One may note that also the region of $|V_{DS}| < |V_{GS} - V_{th}|$ of the transfer characteristics is affected by the geometry of the source insulator overlap. Comparing the images on the right hand side of figure 6.9 reveals the reasons for this: The charge carrier density

[3]For more extracted profiles see appendix B.

at V_{GS} = 1.5 V is almost constant over the entire width of the vertical channel, indicating that the total volume of semiconductor available for charge transport - together with the mobility in this volume - is the limiting factor. In the VOFET without an insulator overlap, a higher charge carrier density is found right at the edge of the source contact due to injection from this vertical edge. This more conductive region results in a significant charge transport path directly at this edge and thus allows for a higher On-state current in comparison to devices with a covered source edge (see figure 6.9 (c)). For the two devices where this vertical source edge is covered it may be observed that charge carriers begin to diffuse into the source-drain overlap region as soon as they are no longer hindered by the source insulator's vertical edge. As is visible from the comparison of figure 6.9 (a) and (b), this diffusion transport begins at a lower position for longer insulator overlap due to its simulated geometry. As a consequence, the lateral extent of the vertical channel is broader for this device than for the one shown in figure 6.9 (b) and thus leads to a slightly higher On-state current in the former device. The difference, however, is very small even for these ideal devices, as can be seen in figure 6.8. A reproduction of this effect in experiments is difficult due to the less ideal shape of the source insulators and the afore-mentioned difficulty in controlling said shape. It must further be expected that such a weak effect would be invisible in comparison to e.g. trapping effects due to variations in sample cleanliness.

REVERSE BIAS

When the positions of the source and drain electrodes inside the VOFET stack are swapped, i.e. the top electrode is used as source and the middle electrode as drain, a similar saturation trend is observed. This is displayed in figure 6.11 for the original VOFET design with a long insulator overlap. The corresponding transfer characteristics for this device are displayed in figure 6.12 together with the reverse bias characteristics of the device with a small insulator overlap. As can be observed from the latter figure, the transfer characteristics in reverse bias condition show no shoulder formation, as charge carriers are now injected directly into the bulk of the vertical channel, rather than forming a narrow channel around the edge of the source insulator. Furthermore, the characteristics saturate at a current density two orders of magnitude lower than that of the original configuration. Figure 6.11 (a) shows that this lower saturation current is due to effective trapping of

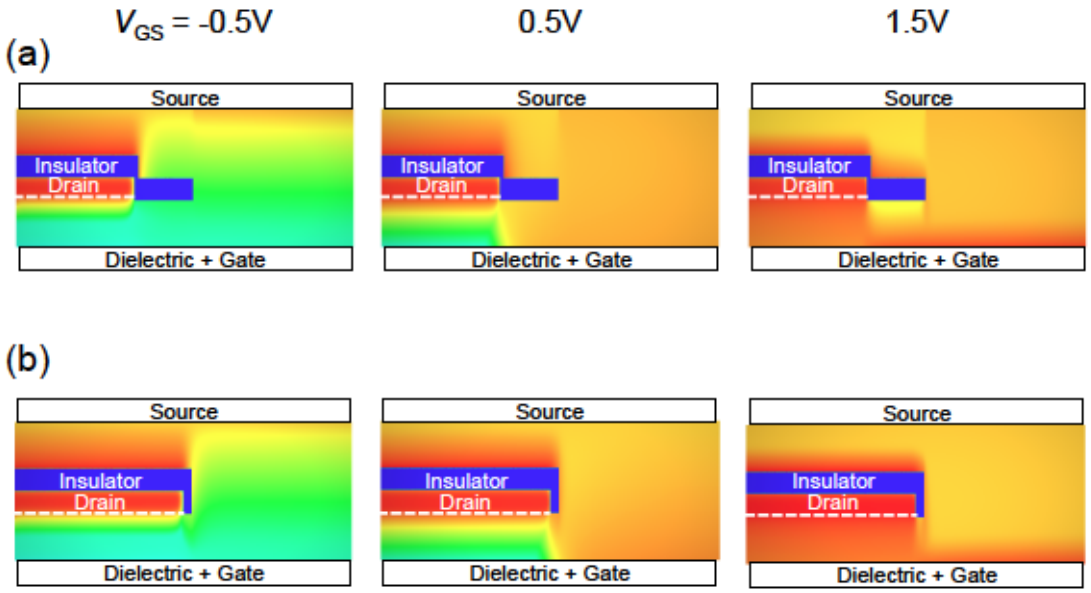


Figure 6.11.: Electron density extracted from the WIAS simulation for the VOFET geometries with short and long insulator overlap at different source-gate biases. The source and drain electrodes have been swapped here. The applied source-drain voltage is 1.0 V.

charge carriers at the source insulator surface, from which they cannot migrate into the vertical channel via diffusion. This effect has also been observed in real devices. Here, however, the difference in On-state currents is less than an order of magnitude (see figure 6.12 (b)), most likely due to the fact that accumulation at the source insulator surface will be less pronounced in the real device, since the insulator here is 100 nm thick and the source-drain field thus much weaker in comparison to the simulation. Furthermore, the smoother geometry of the real insulator may allow for longer diffusion paths by attracting carriers primarily to the thinner parts of the insulator layer which are close to the vertical channel (see figure 6.3 (c)). Leakage currents through pinholes in these thinner regions also have to be considered as the real SiO_2 layer is not an ideal insulator.

This section has provided a concept for the theoretical working mechanism of the VOFET: The majority of charge carriers is injected into the device via the bottom surface of the source electrode. These charge carriers accumulate at the gate dielectric interface and diffuse along this interface in an accumulation layer of only a few nm thickness. For $|V_{DS}| < |V_{GS} - V_{th}|$, the strong gate field accumulates more carriers at the gate dielectric interface than can be transported by the vertical channel under the comparatively weak drain bias. Here, the VOFET is limited by the bulk mobility of the vertical channel as well as its lateral extent. In the VOFET's saturation regime, where $|V_{DS}| > |V_{GS} - V_{th}|$, the

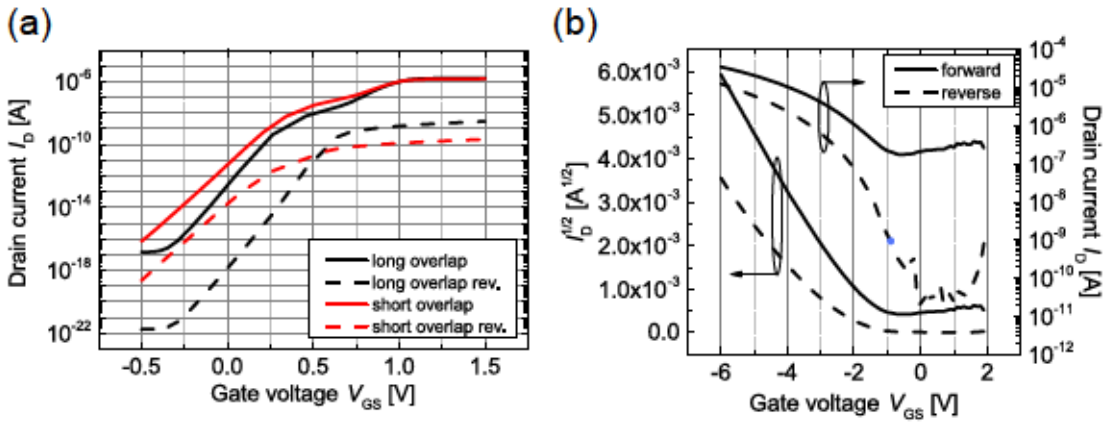


Figure 6.12.: Transfer characteristics of simulated VOFETs (a) and a real pentacene VOFET (b) in forward bias, i.e. with the source electrode in the middle of the stack, and in reverse bias, where the source electrode is on top of the stack. For (a), the applied source-drain voltage is 1.0 V, for (b) it is -6 V.

stronger drain bias produces a more efficient drift transport and so the vertical channel is characterised as a thin region near the source insulator's vertical edge, with a high charge carrier density. In this regime, I_D may be limited by injection into this vertical channel, i.e. by the charge carrier mobility in the accumulation layer near the gate dielectric interface.

6.2. THE VERTICAL CHANNEL

The saturation effect in the transfer characteristics of the simulated device has so far not been observed in experiment. It is questionable therefore whether this is a mere artefact of the simulation, owing to the small lateral extent of the grid, or whether this regime might indeed be reached also in a real device for sufficiently high gate voltages (this also depends on the breakthrough voltage of the gate dielectric). In any case, it seems necessary to compare the vertical channel formation in the simulation to the same process in the real device in order to verify the correctness of the simulation and to get a first idea of how broad the real vertical channel may be. This latter point in particular is important for future circuit implementation as it puts a lower limit to the lateral size of the VOFET and thus to the achievable integration density of this technology.

In a series of papers, Fischer *et al.* discussed Joule heating effects in organic devices [284–286] and demonstrated that thermal imaging can be used to visualise current flow in organic semiconductors under self-heating conditions [284]. However, the work of Fischer

et al. suggests that high current densities of the order 10^4 mA/cm^2 are required in order to reach the self-heating regime in organic layers with a thickness of 100 nm or less. In the VOFET layout shown in table 4.5, the drain electrode is 100 µm wide and the distance between two source contacts is 50 µm. Assuming that indeed this entire area is used to transport current, this gives a current density on the order of 10 mA/cm^2 to 100 mA/cm^2, which is expected to be insufficient for thermal imaging via self-heating. A brief test with the infrared camera setup used by Fischer *et al.* confirmed this assumption.

An alternative approach to visualising the vertical channel formation in the real VOFET has been presented by Nakamura *et al.* [228, 229]: The integration of light-emitting layers into the vertical channel region produces a vertical organic light-emitting transistor (VOLET, see figure 6.13 (a)) whose emission zone - in the ideal case - should be limited to that area of the device in which the vertical channel forms. Indeed, in their first publication, Nakamura *et al.* reported that the emission zone of their transistors was limited to the vicinity of the source contacts, such that dark stripes could be seen between the individual source contacts, which were approximately 200 µm apart [228]. Rather than investigating this effect further, however, Nakamura *et al.* optimised the device towards wide emission zones so as to demonstrate a light-emitting transistor suitable for display and lighting applications without intermediate metal contacts. The basic concept, however, may be used to compare the vertical channel formation in the simulation to the same process in a real device, as the size of the emission zone and the intensity of emitted light can directly be correlated to the lateral size of the vertical channel as well as the charge carrier density inside it for a given bias condition. For this purpose, the exact structure published by Nakamura *et al.* is less suitable due to its reliance on bottom emission through several organic layers and a transparent, yet thick gate electrode and substrate. In contrast, light emitted through the top of that same VOLET architecture would pass only through the emission layer and top electrode and is thus expected to be scattered less, affording a higher lateral resolution for visualising the vertical channel. For such top emission, a thin, transparent drain electrode is required which provides good electrical conductivity and the right work function for electron injection into the underlying organic layers. For such purposes, Schubert *et al.* report excellent performance of Ca:Ag and n-C_{60} electrodes for organic solar cells [287, 288]. Comparable performance has also been reached with a thin Ag electrode, where a closed Ag film of only 9 nm thickness was formed on top of

organics using 3 nm Au as a seed layer [289]. Replacing the VOFET drain electrode by this transparent Ag electrode and exchanging the pentacene layer in the vertical channel for the combination of α-NPD and Alq_3 reported by Nakamura (see figure 6.13 (b)), however, does not lead to the desired light emission, although the electrical characteristics of such a VOLET remain comparable to those of a pentacene VOFET.

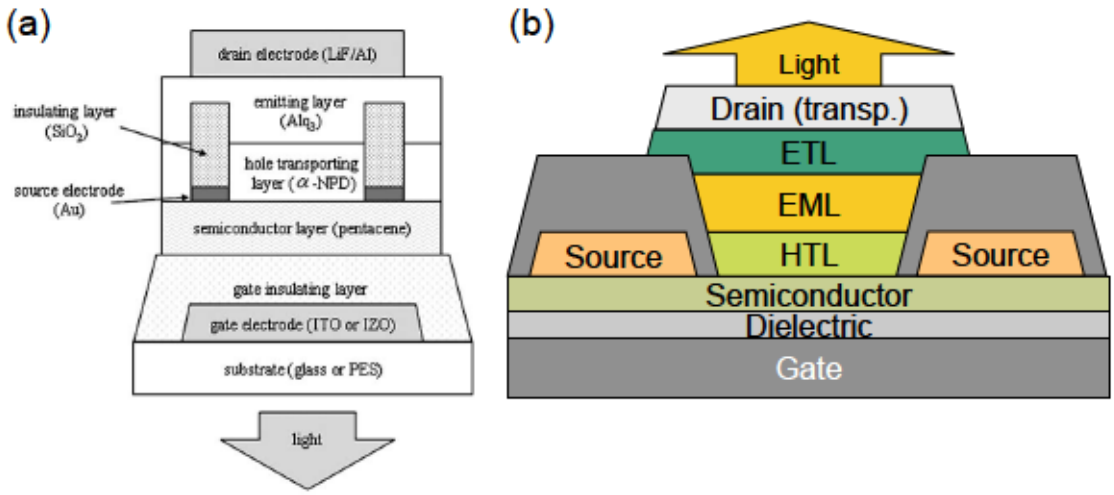


Figure 6.13.: (a) Schematic representation of the original VOLET design by Nakamura *et al.*, reprinted from ref. [228] with permission from AIP Publishing, and (b) the modified structure for top emission through a transparent drain electrode. Here, the acronyms HTL, ETL and EML stand for hole transport layer, electron transport layer and emission layer.

As discussed in more detail in the master thesis of Michael Sawatzki [275], the reasons for the lack of light emission are twofold: For one, the Au seed layer provides a workfunction mismatch with the underlying Alq_3, thus making the OLED stack less efficient. Secondly, electron microscopy on the proposed stack revealed a partial contact of the drain electrode to the bottom pentacene layer due to a fold-up of the source insulator edge during lift-off (observed both for sputtered SiO_2 and particularly strongly for ALD-deposited Al_2O_3). As a noticeable injection barrier must be assumed between pentacene and α-NPD, it is reasonable to assume that the entire OLED stack was bypassed during charge carrier transport through the VOLET (see figure 6.14). The replacement of the oxide source insulator by the insulating polymer OSCoR 4000 (see chapter 5) resolves the latter issue, while a suitable electron-injecting, transparent drain electrode was obtained through combining a 5 nm seed layer of Al with 15 nm Ag (see chapter 5 of ref. [275] for details). Through separate optimisation of the OLED with regards to maximum light intensity and spatial resolution (see chapter 5 of ref. [275] for details), the VOLET stack shown in figure

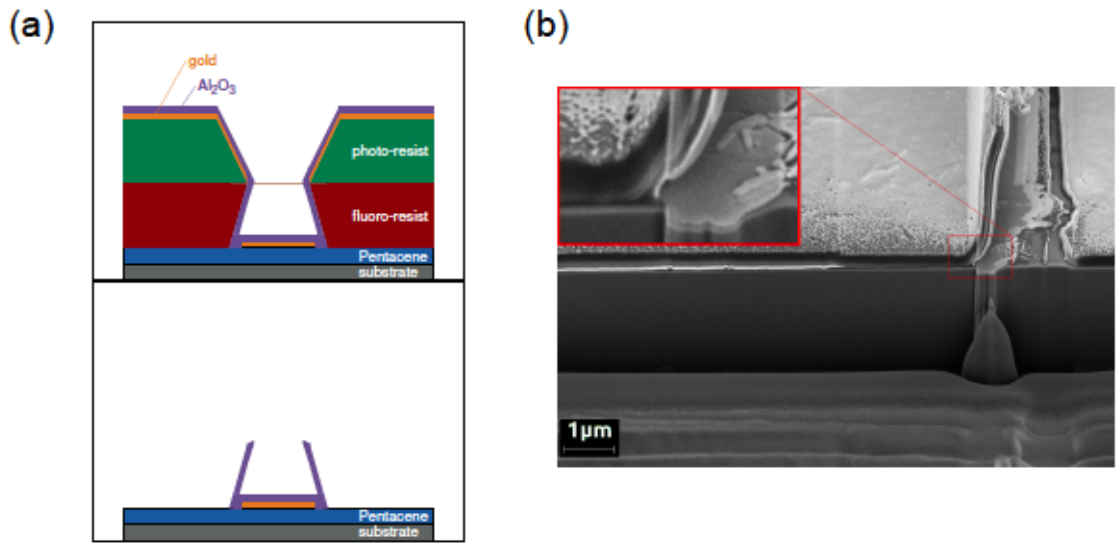


Figure 6.14.: (a) Schematic representation of the formation of a vertical insulator edge after photoresist lift-off due to ALD processing. (b) SEM image of the folded-up edge of a VOFET source insulator. Figures were taken from ref. [275].

6.15 was finally determined to be the best trade-off between good electrical performance, high spatial resolution in the vertical channel and sufficient light intensity for imaging.

Light emission from this stack was obtained by biasing it under the same conditions as detailed in chapter 4, with light intensity measurements at different bias conditions obtained by a high-resolution microscope-video system (see chapter 3 of ref. [275] for details). Figure 6.16 shows the measured light intensity distribution between the two source contacts of the VOLET (spaced 100µm apart) as a function of gate and drain bias. In these measurements, only one source contact is grounded, while the other is kept floating, so as to be able to observe the vertical channel formation originating from only one source contact.

The obtained data clearly compares qualitatively to the simulation data shown in the previous section. For $|V_{DS}| > |V_{GS} - V_{th}|$, the emission zone, and thus the vertical channel, is confined to the vicinity of the source edge, with light intensity and thus charge carrier density dropping rapidly towards the bulk of the semiconductor. As the gate bias is increased to approach the regime $|V_{DS}| < |V_{GS} - V_{th}|$, the emission zone broadens considerably and almost approaches the edge of the floating source contact[4]. Furthermore, a

[4]The breakthrough field of Al_2O_3 is often quoted to be in the range of 4 MV/cm, giving a breakdown voltage somewhere in the range of 10 V to 15 V for the gate dielectrics used here. Since V_{th} is high due to the additional energy barriers in the vertical channel and high currents and thus high V_{DS} is required to obtain sufficient light emission for imaging, actually driving the VOLET fully into the regime $|V_{GS} - V_{th}| > |V_{DS}|$ is difficult and was avoided here so as not to damage the samples.

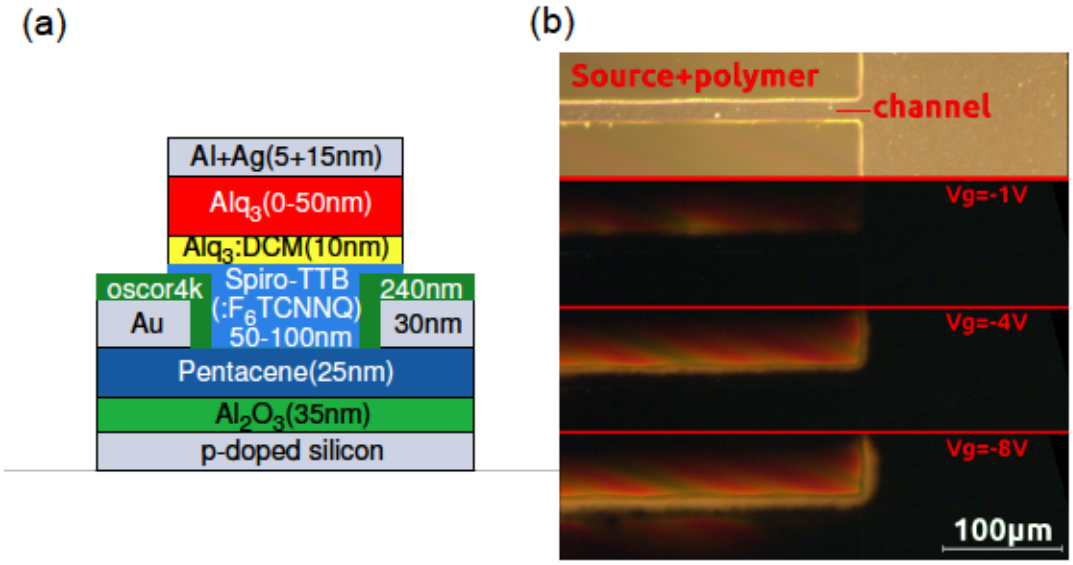


Figure 6.15.: (a) Optimised VOLET stack as proposed by Michael Sawatzki and (b) light emission obtained from this stack as a function of gate voltage. The top section of this image shows the VOLET without current flow under external illumination. Figure taken from ref. [275].

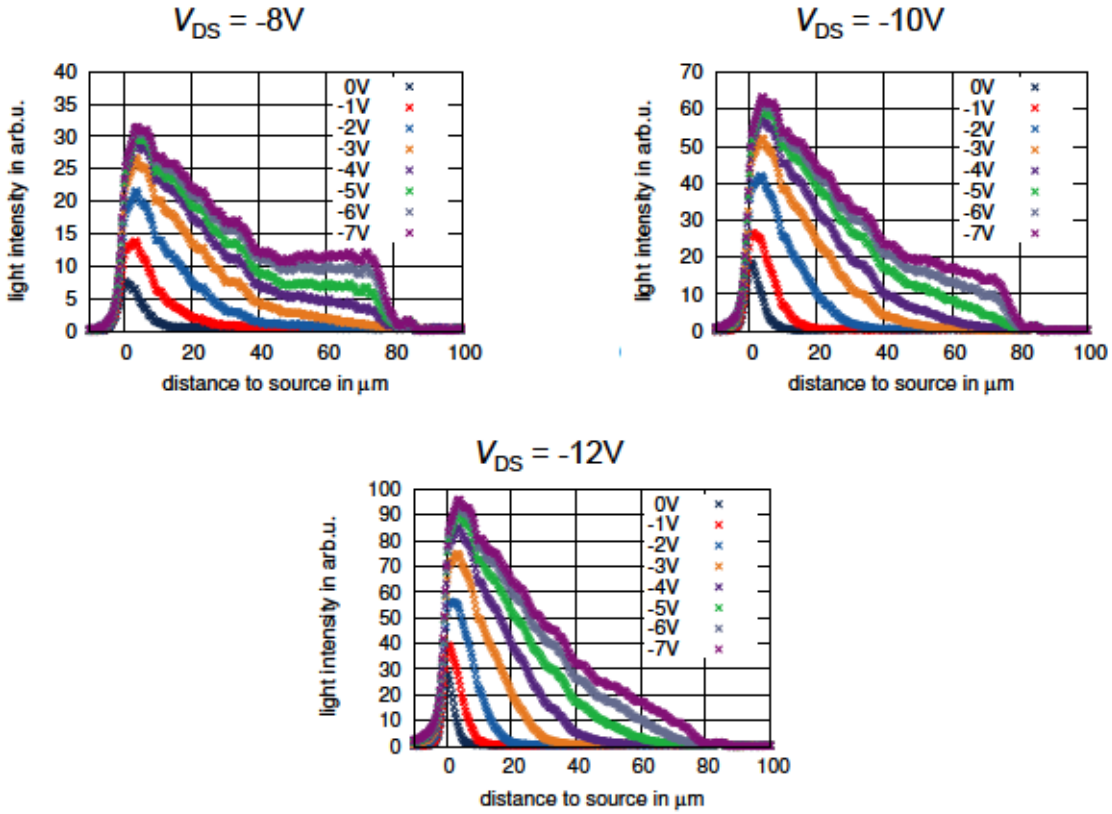


Figure 6.16.: Light intensity distribution in the VOLET as a function of gate bias for different drain voltages. Figure taken from ref. [275].

plateau of constant light intensity / charge carrier density begins to form in a manner similar to that observed in the simulation. This broadening effect is aided further by the injection barrier between the hole accumulation layer in the pentacene and the Spiro-TTB acting as hole transport layer for the OLED stack. Reducing this injection barrier by p-doping the Spiro-TTB with F_6-TCNNQ consequently causes the formation of an overall narrower channel under the same bias conditions (see figure 6.17 (a)). Equally, an increase of the layer thickness of Alq_3 leads to a broadening of the emission zone due to the effectively lowered source-drain field (see figure 6.17 (b)) and the stronger accumulation of holes at the emission layer interface in comparison to electron accumulation.

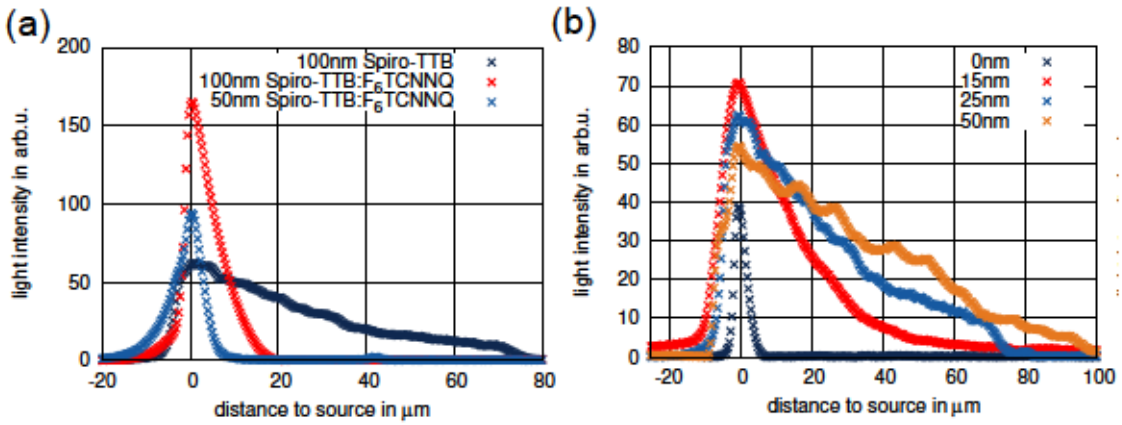


Figure 6.17.: (a) Light intensity distribution inside VOLETs with 25 nm Alq_3 and varying thicknesses of doped Spiro-TTB. (b) Light intensity distribution inside VOLETs with 100 nm Spiro-TTB and varying thicknesses of Alq_3. The applied drain and gate voltages are V_{DS} = -10 V and V_{GS} = -6 V in both cases. Figures were taken from ref. [275].

Some peculiar features of this architecture were also found and are illustrated in figure 6.18: The use of a transparent polymer as source insulator next to the vertical edge of the emission zone may lead to light trapping and subsequent wave guiding inside this polymer for certain polymer layer thicknesses (see figure 6.18 (a)). This effect might be utilised for device applications of the VOLET so as to broaden the emission area. Furthermore, a misalignment of the individual OLED layers may lead to multi-colour emission, as all three layers may be excited under certain bias conditions (see photograph in figure 6.18 (b)). Again, exploiting this fact for applications could provide an alternative to separate RGB colour OLEDs in AMOLED displays or similar. Thirdly, by keeping one of the source contacts floating and increasing the gate bias sufficiently, the formation of a second, albeit

weaker vertical channel in the vicinity of this second source contact was observed (see figure 6.18 (b)). The origins of this last effect are not quite clear yet, but may also be exploited to broaden the VOLET's emission zone for display or lighting applications.

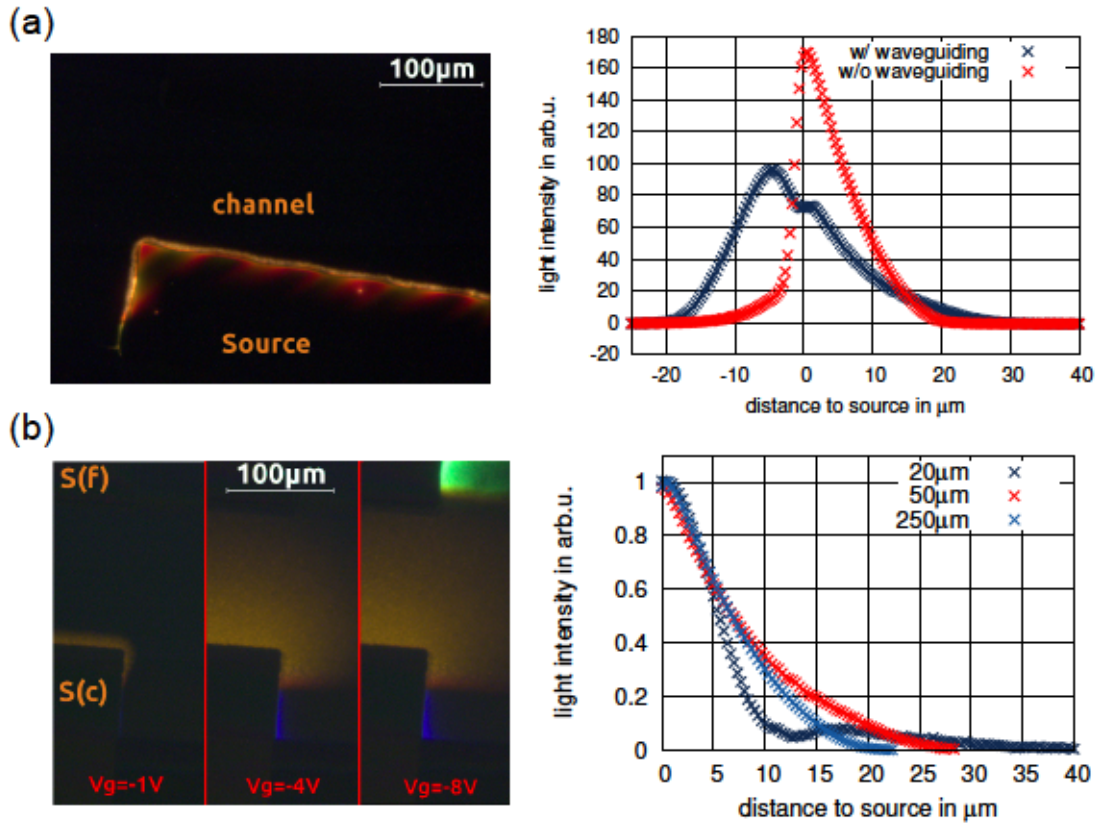


Figure 6.18.: (a) Microscope image of light emission from a VOLET with wave guiding effects in the OSCoR layer (left) and light intensity distribution with and without wave guiding effects. The microscope image shows different intensities of guided light along the source insulator edge due to a slight variation in polymer layer thickness. (b) Microscope image of a VOLET with two source contacts (spaced 100 µm apart)at different gate bias conditions. Here, S(c) indicates the connected source, while S(f) represents the floating source. Yellow light emission is obtained from the Alq_3:DCM layer, green emission stems from pure Alq_3 and blue emission is caused by Spiro-TTB. On the right is shown the light intensity distribution for different distances of the connected and floating source. Short distances allow more easily for charging and thus emission at the floating source. Figures were taken from ref. [275].

While the power conversion efficiency of the VOLET stack discussed here does of course not compare favourably to that of a state-of-the-art OLED (see chapter 5 of ref. [275]) , its performance may be improved to a competitive level by introducing a more efficient OLED stack. For the purpose of this work, the device has proven to be a useful tool to visualise the vertical channel formation in the VOFET architecture for the first time. In the pure pentacene or C_{60} VOFET, the formation will of course be somewhat different and

tend more strongly towards the locally confined channel near the source edges due to the lack of high injection barriers in the vertical channel. Yet it was possible to demonstrate experimentally that for the right bias conditions, a strong channel broadening as predicted by the simulation may indeed be achieved. This suggests that if both source contacts of the VOFET are connected and inject charge carriers into the device, which diffuse along the gate dielectric very efficiently, the overall current transport may be similar to that predicted by Ben-Sasson *et al.* for the OSBT [202, 203], i.e. in the regime $|V_{DS}| < |V_{GS} - V_{th}|$, the accumulation layer may be treated as a virtual contact, while transport through the vertical channel approaches the SCLC regime. However, in order to know more precisely under which bias conditions such scenarios are possible in the real device, it is vital to understand the injection and transport properties of the material stack at hand. For the case of the VOFETs discussed in this thesis, this requires in-depth knowledge particularly of the hole and electron injection properties of Au into pentacene and C_{60}, as well as the transport properties of the intrinsic semiconductors. For the case of C_{60} as a symmetrical molecule, it is easy to show that the charge carrier mobility is isotropic and its value depends mostly on the quality of the deposited film (for average values see table 4.1). Electron injection, while not very efficient, is also possible from Au (see ref. [90, 230]), but may indeed be the limiting factor in C_{60} VOFETs when trying to achieve a fully saturated channel. For the case of pentacene as a polycrystalline material, the matter of charge carrier transport in particular is somewhat more complex and will therefore be discussed in the next section.

6.3. CHARGE TRANSPORT IN PENTACENE[5]

Pentacene is one of the most commonly used materials in organic electronic devices, especially in organic field-effect transistors (OFETs) [8, 82, 104, 113, 160, 290–292], due to the good transport properties along the crystal *a-b* plane [293–296], which typically orientates in parallel to the substrate surface in conventional bottom-gate OFET structures with oxide dielectrics [297, 298]. The effective hole mobility in this *a-b* plane has previously been the subject of intensive study, along with its dependence on pentacene film morphology [84, 160, 232, 290, 299–303]. So far, however, only a few studies concerned the transport perpendicular to the *a-b* plane [293–295, 304] or more generally in the bulk phase of pentacene, as transport in this regime has never been of much interest in real

[5]Most of the text and figures in this section have been published in ref. [231].

devices. With the development of vertical transistor structures however, a more complete understanding of the hole mobility in pentacene and its dependence on film morphology are evidently required, as pentacene VOFETs will rely also on transport perpendicular to the *a-b* plane and through the bulk of the semiconductor (see e.g. figure 6.1, where the top pentacene layer in the vertical channel clearly shows a bulk phase).

Transport in the *a-b* plane of the thin film phase can be investigated by the conventional field-effect mobility measurement in OFET devices, as already demonstrated in the previous chapter. The mobility of the bulk phase of pentacene is tested by the method of electric potential mapping by thickness variation (POEM) [273], which was explained in chapter 4.

For the POEM analysis of the out-of-plane pentacene mobility (which, for VOFET samples, is perpendicular to the substrate surface), a series of p-i-p devices is fabricated on pre-cleaned glass substrates. These p-i-p devices consist of Al top and bottom electrodes and 50 nm-thick injection layers of pentacene, p-doped with F_6-TCNNQ in a doping concentration of 1.5 wt% to ensure a low injection barrier and the formation of an SCLC regime, while at the same time leaving the morphology of pentacene unaltered [247]. Between the injection layers, intrinsic pentacene is deposited with varying thickness from 30 nm to 250 nm (see figure 6.19 for a device schematic).

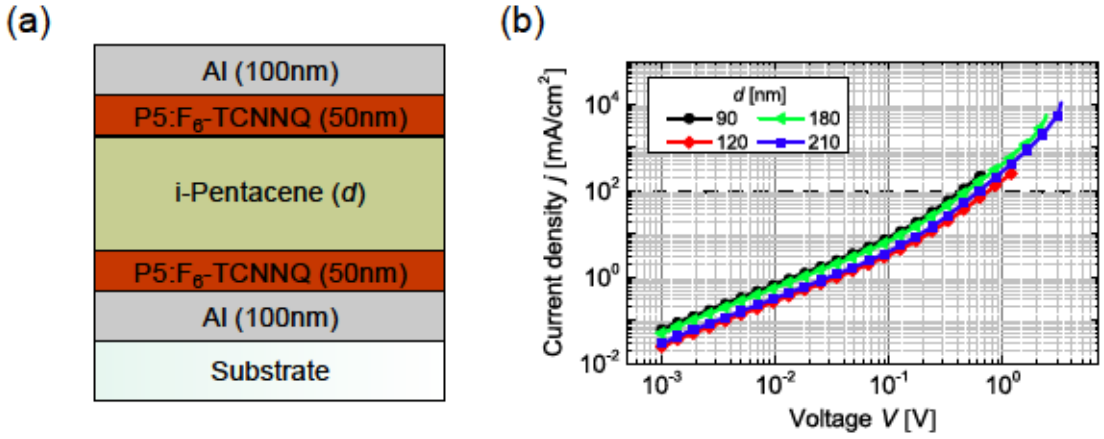


Figure 6.19.: (a) Device schematic of a p-i-p stack for POEM measurements. (b) *jV* characteristics of a series of p-i-p devices with varying intrinsic pentacene thicknesses, deposited at a rate of 2.5 Å/s. The dashed line indicates the current density at which mobility values will be extracted.

The specific layer thickness and low doping ratio for the injection layers are chosen because they provide sufficient improvement of the hole injection into the intrinsic layer[6], so that morphological changes in the intrinsic pentacene due to the p-layer may be excluded. Individual data sets are obtained in this manner for deposition rates of 0.5 Å/s, 1.5 Å/s, 2.5 Å/s and 10 Å/s of the intrinsic pentacene layers, so that the effect of the deposition rate on the hole mobility perpendicular to the substrate can be observed. In order to correlate the mobility values obtained via POEM directly to the in-plane field-effect mobility obtained for pentacene at the same deposition rates, OFET devices are manufactured separately on silicon substrates with 30 nm of Al_2O_3. The contacts are patterned lithographically to form OFETs with a channel width W of 770 µm and channel lengths L of 10 µm, 25 µm, 50 µm and 100 µm (see Fig. 6.21 for a device schematic). As in the previous chapter, the morphology of the 30 nm-thick pentacene films in the OFETs is checked via AFM.

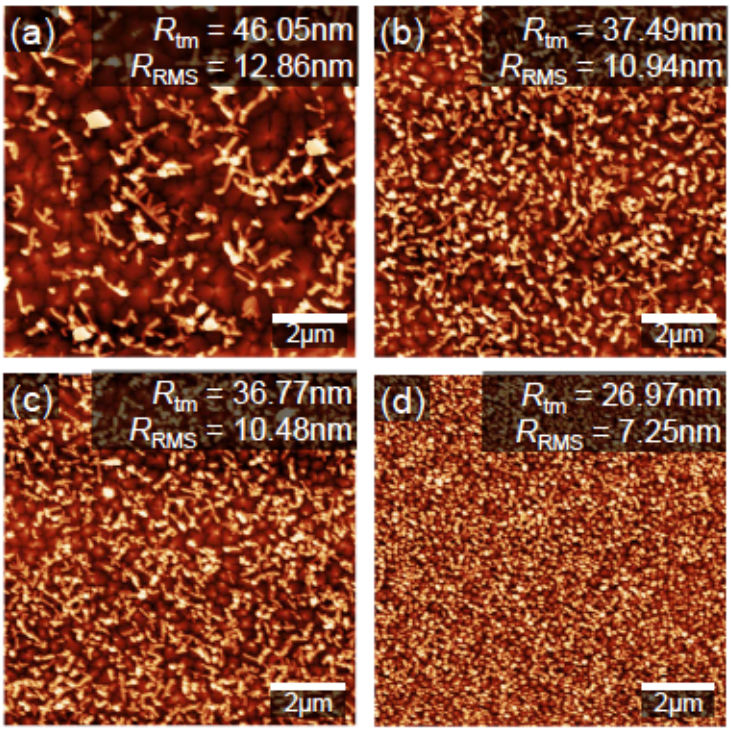


Figure 6.20.: Tapping mode AFM scans of 20 nm-thick P5 films deposited onto 30 nm of $Al_2O_3$with deposition rates of 0.5 Å/s (a), 1.5 Å/s (b), 2.5 Å/s (c) and 10 Å/s (d). The scan areas have a size of 10x10 µm^2 and the RMS roughnesses R_{RMS} and mean peak-to-valley distance R_{tm} are indicated for each sample.

Examining the film morphology of pentacene for the different deposition rates, one observes the onset of pentacene's bulk phase and underneath the dendritic grain structures

[6]Electron injection is suppressed by the dopant, thus affording single carrier devices.

typical for pentacene molecules in the thin film phase stacking vertically on an inert, flat substrate [298]. A distinct transition from large crystal grains at the lowest deposition rate to smaller grains at higher deposition rates is found, as illustrated in figure 6.20. This decrease in lateral grain size goes hand in hand with a noticeable decrease in the average peak-to-valley distance, suggesting a change of grain size in the direction perpendicular to the substrate surface also.

Figure 6.21 shows the field-effect mobility determined for each pentacene deposition rate. The mobility is extracted from the transfer curves of the respective OFETs in saturation mode and from the output characteristics in the linear mode (V_{DS} = -6 V for saturation, V_{DS} = -1 V for linear regime, V_{GS} is swept from 2 V to -6 V) using equations 2.17 and 2.18. Mobility values are obtained for each of the transistor channel lengths indicated above. Figure 6.21 represents the average trend over all devices, with at least two devices measured per channel length. Even the shortest channel devices investigated here show linear behaviour for small drain voltages, so it is safe to assume that contact effects due to non-ohmic injection [102, 113] play only a minor role for the effective mobility values determined here. The observed decrease in mobility is thus likely caused by the increased number of grain boundaries in the conductive channel, as previously observed in similar experiments [160, 232, 290]. This assumption is supported by the fact that the effect of evaporation rate and morphology is slightly more pronounced in the saturation regime, where transport through a region similar to the MOSFET pinch-off [30] may be more obviously affected by the film morphology than the channel region with high charge carrier density.

To determine whether a similar effect can be observed for the transport direction perpendicular to the substrate plane, the *jV* characteristics of four sets of p-i-p devices are measured, each set with an intrinsic pentacene layer thickness varying between 30 nm and 250 nm (in steps of 10 nm up to d = 130 nm, then in steps of 30 nm).

By following the POEM approach as detailed in chapter 4, a map of the applied voltage V as a function of intrinsic layer thickness d is obtained. Figure 6.22 shows this extracted voltage for a current density j of 100 mA/cm^2 for each of the investigated deposition rates. As can be seen from the top graph in this figure, the voltage required to achieve j is an order of magnitude higher for the two lower deposition rates. This difference may be caused by a change in injection barrier due to changing energetic disorder of the films, but

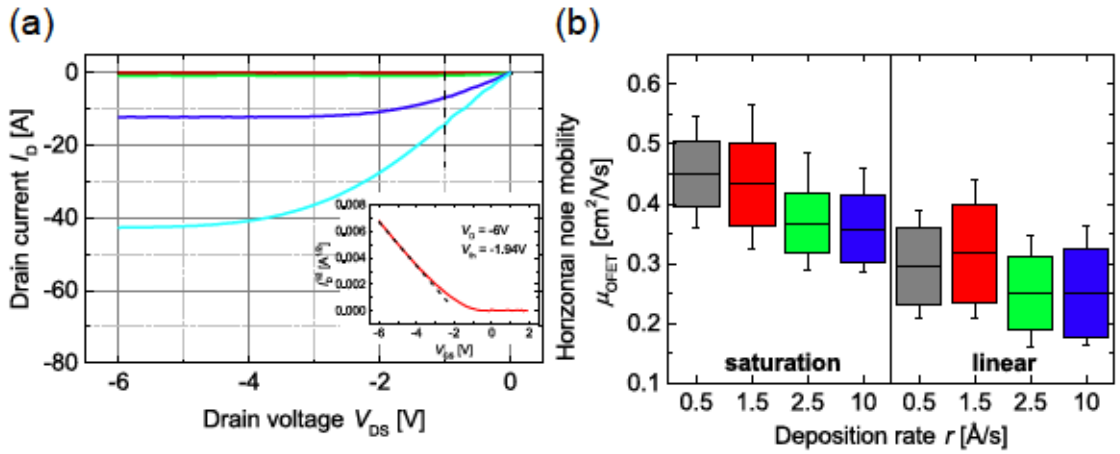


Figure 6.21.: a) Exemplary output and transfer (inset) characteristics of an OFET with L = 25 µm. Dashed lines indicate the positions at which the linear and saturation mobilities are determined from the output and transfer characteristics. b) Effective hole mobilities in the linear and saturation regimes of P5 OFETs with different deposition rates. The whiskers on this box plot denote the range of 1.5 standard deviations, the box area indicates the range of 25% to 75% of the mobility distribution and the central horizontal line of each box shows the mean value of the mobility distribution. For each deposition rate, at least eight devices have been measured.

could equally be attributed to a simple experimental error during sample fabrication. As the subsequent steps of the POEM method require $\partial\Phi/\partial x$ rather than $\Phi(x)$, this effect, which is expected to be independent of d for a given j, is of no consequence for the further analysis. A smoothing algorithm employing Bézier curves is applied to the *V(d)* data, leading to equally spaced data points in F, n and μ as well a reduced range of d remaining for further analysis. From the smoothed field and carrier density distributions the resultant SCLC mobility is finally calculated using the transport equ. 1.12.

As typical for POEM data in this range of μ, the resolution of n is limited. This is observed in figure 6.22 by the lack of decrease in n with increasing d, as would normally be expected. This is an artefact of possible experimental inaccuracies of d as well as of the applied smoothing algorithm and reflects the resolution limit of this POEM data. Nevertheless it is possible to reliably extract average values for the hole mobility perpendicular to the *a-b* plane as a function of the deposition rate used during the evaporation process. These are summarised in figure 6.23.

What is evident from figure 6.23 is a dependence on the deposition rate of the pentacene layer: For the lowest deposition rate, an average hole mobility of approximately 0.012 cm^2/Vs is extracted, while for higher deposition rates, this value decreases and

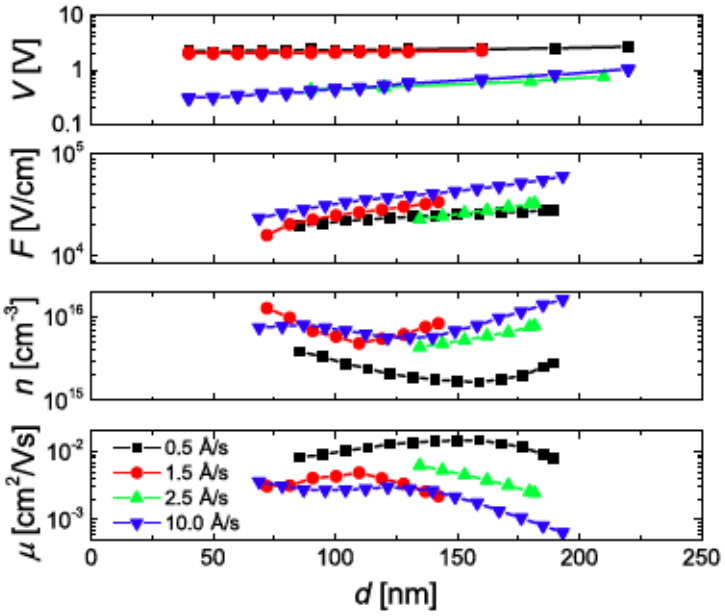


Figure 6.22.: Voltage (V), electric field distribution (F), charge carrier density (n) and mobility (μ) extracted for a constant current density of $j = 100\,\mathrm{mA/cm^2}$ versus intrinsic pentacene thickness d in p-i-p devices.

saturates at approximately $0.003\,\mathrm{cm^2/Vs}$. This result corresponds well to a similar measurement performed by McCarthy *et al.* [304] and is somewhat higher than the mobility determined on ITO [302]. In both cases, a pentacene deposition rate of 1.0 Å/s was used and the Mott-Gurney law was applied to extract the effective pentacene mobility of a single m-i-m structure. Allowing for minor differences in the deposition conditions and pentacene batches used for the respective experiments, one may conclude that for the case of m-i-m devices with moderate charge carrier densities and applied fields, it is reasonable to assume a constant hole mobility, which - for metallic injecting contacts - should be in the region of $0.005\,\mathrm{cm^2/Vs}$ to $0.01\,\mathrm{cm^2/Vs}$ and thus one to two orders of magnitude below the determined field-effect mobility for the *a-b* plane. This finding is also in accordance with previous studies, which did not calculate the exact values of mobility, but did suggest a directional dependence of the mobility based on conductivity measurements [293, 295]. It is further evident that the evaporation conditions affect the morphology and thus the hole mobility of pentacene not only in the hitherto investigated *a-b* plane transport, but also perpendicular to this plane and must thus be considered when fabricating diode or VOFET devices. A clear n- or F-dependence of μ, as previously observed for transport in the *a-b* plane [296, 301], can not be extracted from this data as variations in μ with varying j are in the range of the uncertainty limit of this POEM series. This suggests that the constant

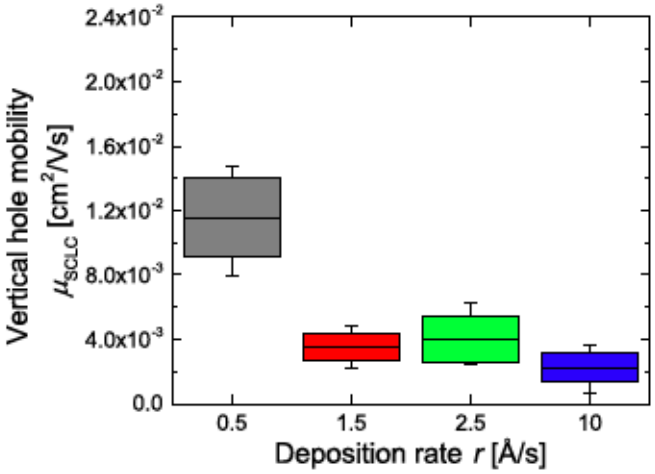


Figure 6.23.: SCLC mobility extracted for each evaporation rate at a constant current density of $j = 100\,\mathrm{mA/cm^2}$. The box chart is defined in the same way as figure 6.21.

mobility assumed for simulations is indeed a viable assumption for the purpose of this thesis, provided that the regime of charge carrier densities present in the VOFET does not show a grossly different trend for μ.

6.4. EFFECTS OF MOBILITY AND LAYER THICKNESS IN PENTACENE VOFETS

The previous section has highlighted the importance of an in-depth knowledge of the properties of polycrystalline materials such as pentacene. The ability to vary the anisotropic charge carrier mobility through the deposition parameters may prove a useful tool in tailoring electronic device properties to a specific application. Some effects of this mobility variation have already been visible in chapter 5: A variation of mobility in the lower pentacene layer (where diffusion transport in the accumulation layer is dominant) affects the output characteristics of the VOFET, but its effects may be overshadowed by experimental artefacts such as a changing channel or contact resistance due to photoresist residuals. From the field-effect mobilities determined in the previous section, it seems clear that this diffusion transport is efficient even on the length scale of µm and perhaps comparable to that in a top-contact OFET. The question therefore arises how the bulk mobility in the nm-long vertical channel affects the overall transport properties of the device and whether variations in the bulk mobility are at all visible in the device performance.

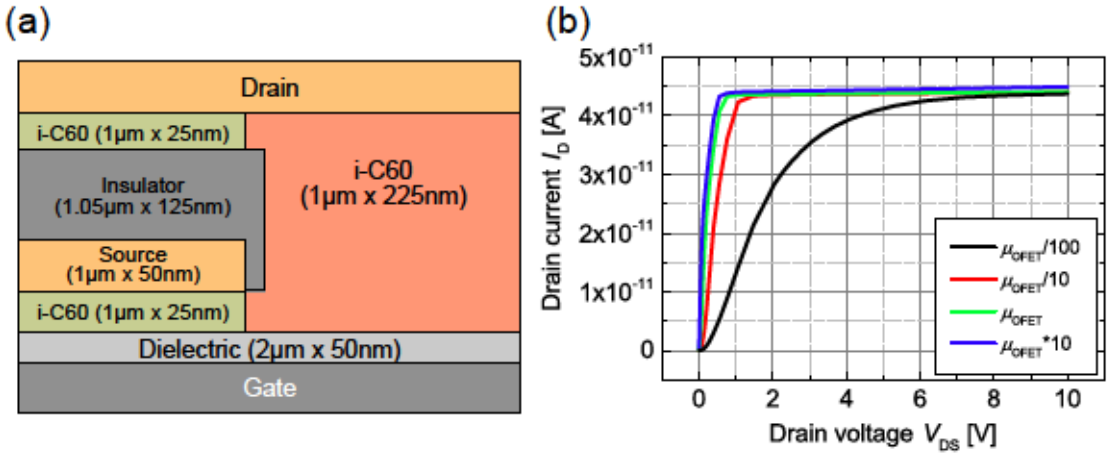


Figure 6.24.: Schematic representation (a) and output characteristics (b) of a simulated C_{60} VOFET with a 50 nm source insulator overlap at a gate bias of 2 V. The C_{60} layers indicated in green are kept at a constant mobility of μ_{OFET} = 0.1 cm^2/Vs as before, while the mobility in the vertical channel region (indicated in red) is varied. Electron density distributions for these devices are shown in figure 6.25.

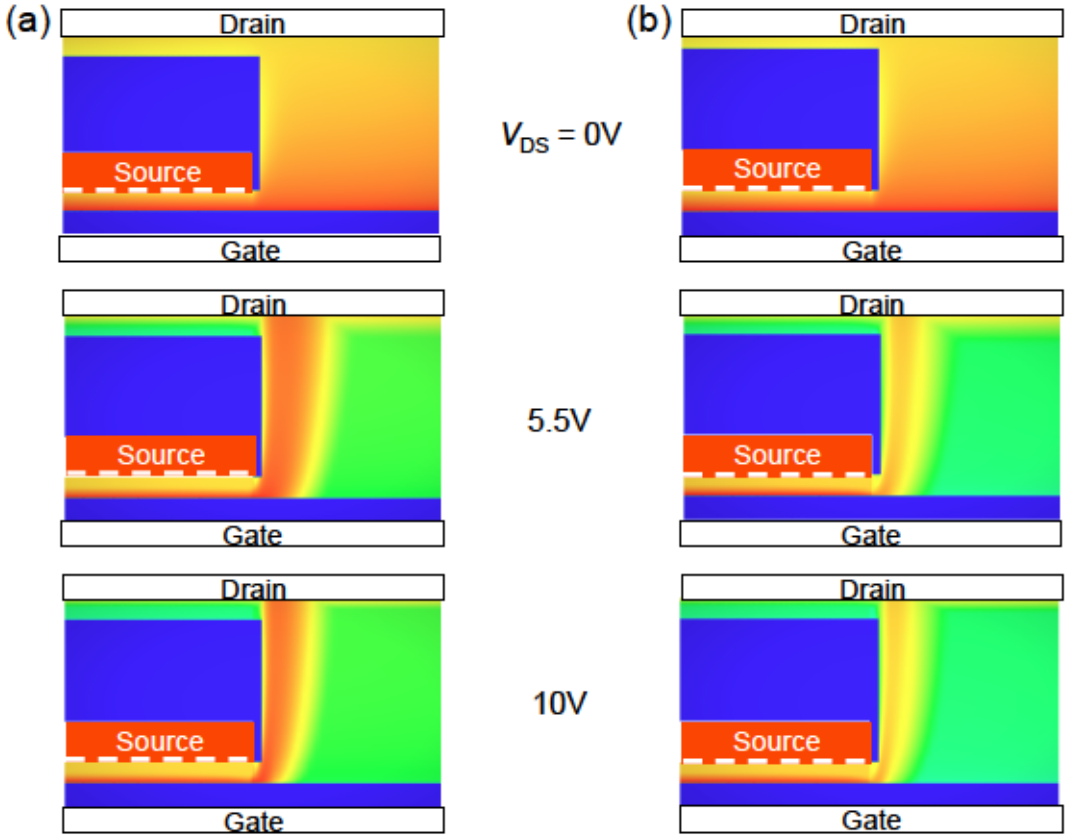


Figure 6.25.: Simulated electron density distributions for the VOFETs shown in figure 6.24 at different drain bias conditions: (a) the device with the smallest channel mobility of 0.01μ_{OFET} and (b) the device with the highest mobility of 10μ_{OFET}.

Although the previous section has suggested a certain amount of control over the bulk mobility of pentacene via the evaporation rate, studying the effects of bulk mobility variation may more easily be done via simulations as the mobility range accessible here is virtually unlimited and there are no reproducibility issues. Figure 6.24 shows the output characteristics of simulated devices with a varying bulk mobility in the vertical channel at V_{GS} = 2 V. These output characteristics may be separated into three distinct regions: A non-linear regime at very small V_{DS}(truly visible only for the lowest mobility in figure 6.24 (b)), a linear regime for moderate V_{DS} and a saturation regime for large V_{DS}. Non-linear regimes at small V_{DS} would, in a real device, typically be associated with a non-ohmic injection due to Schottky barriers at the contacts. As such a Schottky barrier has not yet been included in the simulation, the non-linearity must arise from transport. Indeed, it is found that for a given I_D in this regime, there is a linear relationship between V_{DS}^2 and the inverse of the effective bulk mobility in the channel, denoted as μ_{eff}. This is illustrated in figure 6.26 and suggests a limitation of I_D by an SCLC regime [271][7]. Similarly, the linear

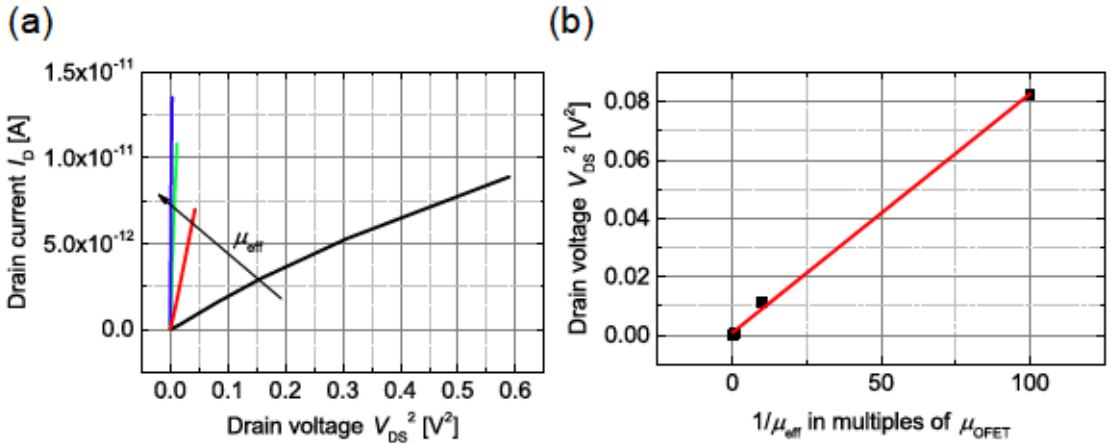


Figure 6.26.: (a) Simulated I_D versus V_{DS}^2 for small V_{DS}, with colour coding as in figure 6.24. (b) Linear relationship between V_{DS}^2 and $1/\mu_{eff}$ for a fixed I_D of approximately 1.5×10^{-12} A.

and saturation regimes show a strong / weak linear dependence on V_{DS}, as expected for OFETs from the gradual channel approximation (see chapter 2). If the gradual channel approximation is applicable here, then there should be a linear relationship between the gradients of the output characteristics and μ_{eff} in these two regimes. Such a fit has been attempted in figures 6.27 and 6.28, however the trend is not clear.

[7]Note that the slight deviations from the straight line are an artefact of the simulation: data points were not always produced at exactly the same I_D, so the closest neighbouring points were chosen instead.

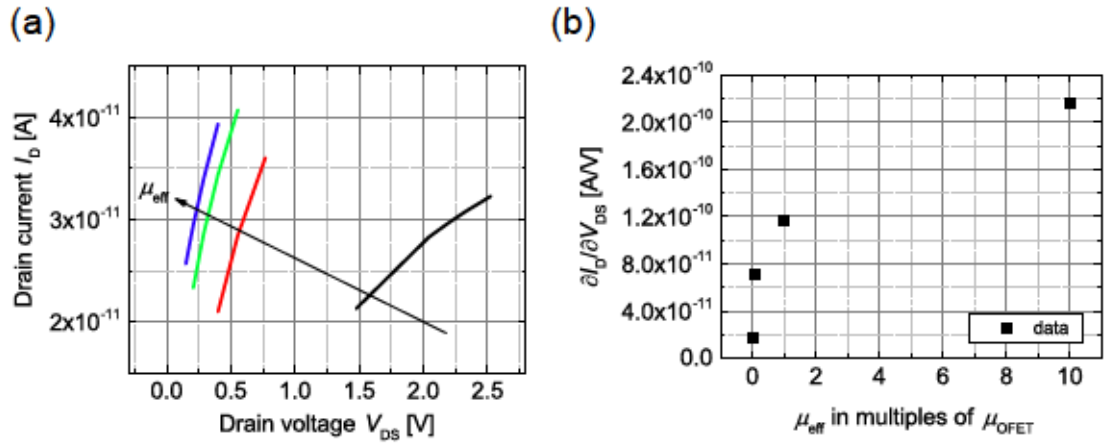


Figure 6.27.: (a) Simulated I_D versus V_{DS} for moderate V_{DS}, with colour coding as in figure 6.24. (b) Linear relationship between the gradient of the output characteristics in (a) and μ_{eff}.

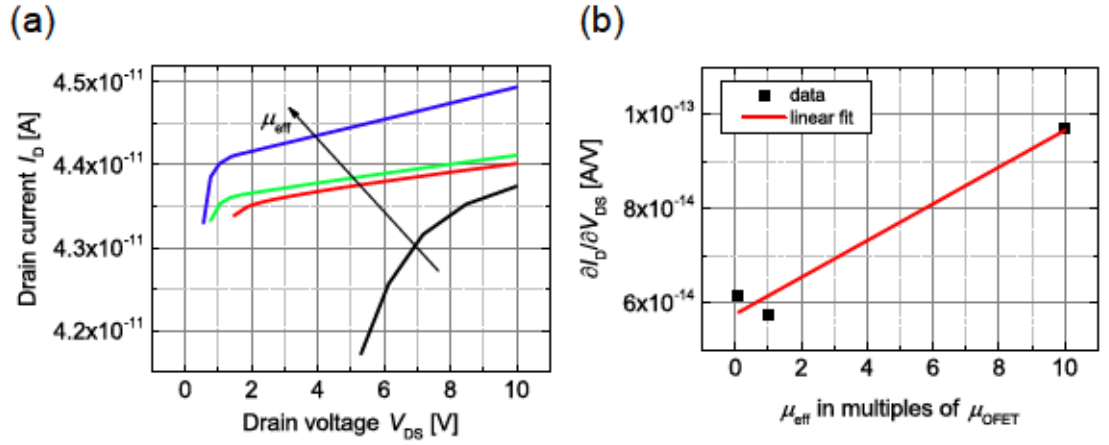


Figure 6.28.: (a) Simulated I_D versus V_{DS} for high V_{DS}, with colour coding as in figure 6.24. (b) Linear relationship between the gradient of the output characteristics in (a) and μ_{eff}.

For the linear regime, this may be due to the fact that there is only a small transition region between the SCLC regime and the saturation regime, for which the simulation does not provide many data points. The uncertainty in the calculated gradients is therefore considerable. For the case of the saturation regime it may be noted that a clear saturation does not even form for the lowest mobility value investigated here, thus a data point in figure 6.28 (b) is missing for this mobility value, which might have clarified the trend somewhat.

Another approach to determine whether trends similar to the gradual channel approximation are present in the VOFET[8] is to vary the vertical channel's layer thickness rather than the mobility.

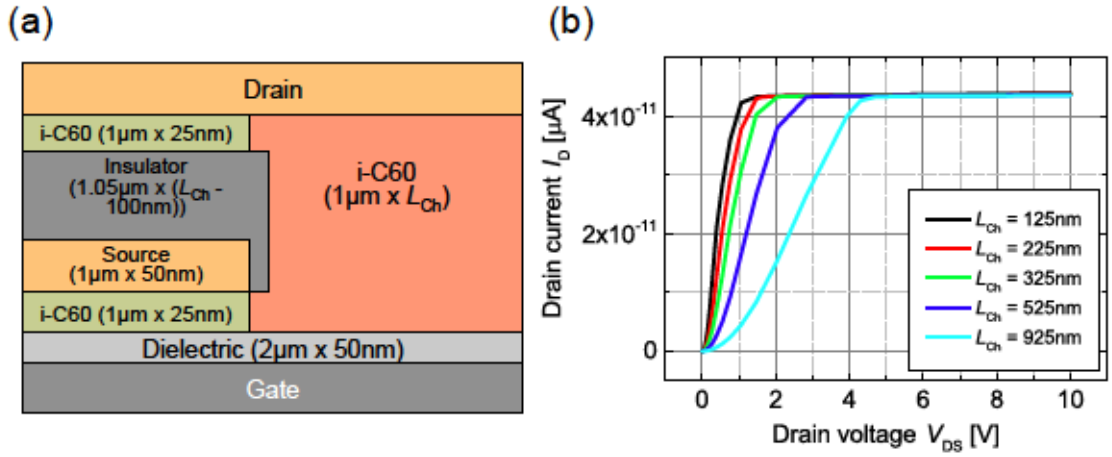


Figure 6.29.: Schematic representation (a) and output characteristics (b) of a simulated C_{60} VOFET with a 50 nm source insulator overlap at a gate bias of 2 V. All C_{60} layers are kept at a constant mobility of μ_{OFET} = 0.01 cm^2/Vs, while the thickness of the bulk C_{60} (indicated in red) is varied along with the source insulator thickness. Electron density distributions for these devices are shown in figure 6.30.

This is demonstrated in figure 6.29 for a series of simulated devices. The same kind of analysis of the output characteristics as before may be performed on these simulated devices, as they, too, can be separated into a non-linear, a linear and a saturation regime. Figures 6.31 to 6.33 show the output characteristics in these separate regimes together with the extracted dependencies on the bulk layer thickness L_{Ch}. Again, a certain amount of error has to be allowed in the linear fitting due to the amount of data points provided by the simulation, particularly in the regime of moderate V_{DS}. The good fit of V_{DS}^2 to L_{Ch}^3 in figure 6.31 confirms the formation of an SCLC current in this non-linear regime of

[8]This would allow for a description of the VOFET by the gradual channel formalism and thus provide an easy approximation of standard transistor parameters such as average mobility from these standard equations.

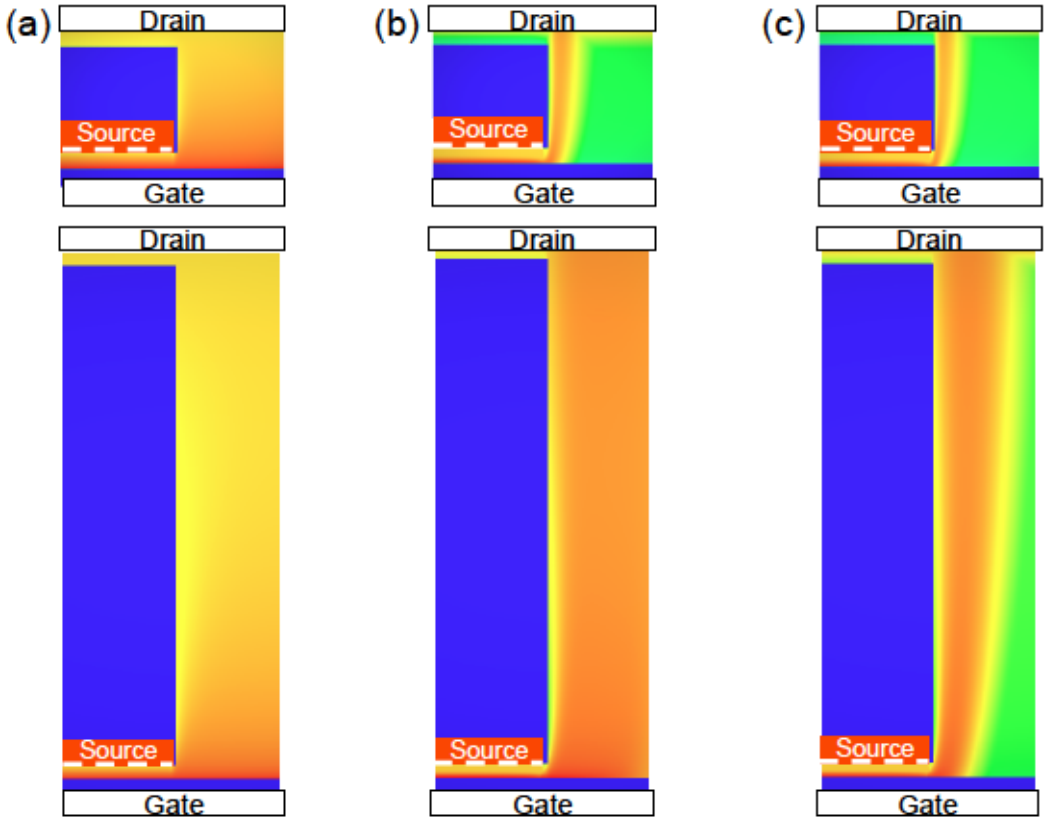


Figure 6.30.: Simulated electron density distributions for the VOFETs shown in figure 6.29 at drain voltages of 0 V (a), 5.5 V (b) and 10 V (c). The top device in each panel is the one with the smallest channel layer thickness of 125 nm, the bottom device is the one with the largest thickness of 925 nm.

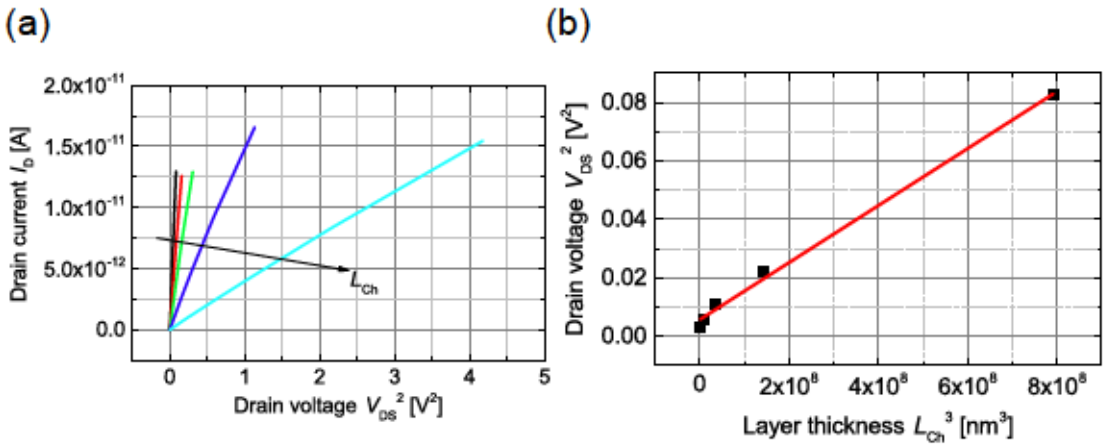


Figure 6.31.: (a) Simulated I_D versus V_{DS}^2 for small V_{DS}, with colour coding as in figure 6.29. (b) Linear relationship between V_{DS}^2 and $1/L_{Ch}^3$ for a fixed I_D of approximately 1.5x10^{-12} A.

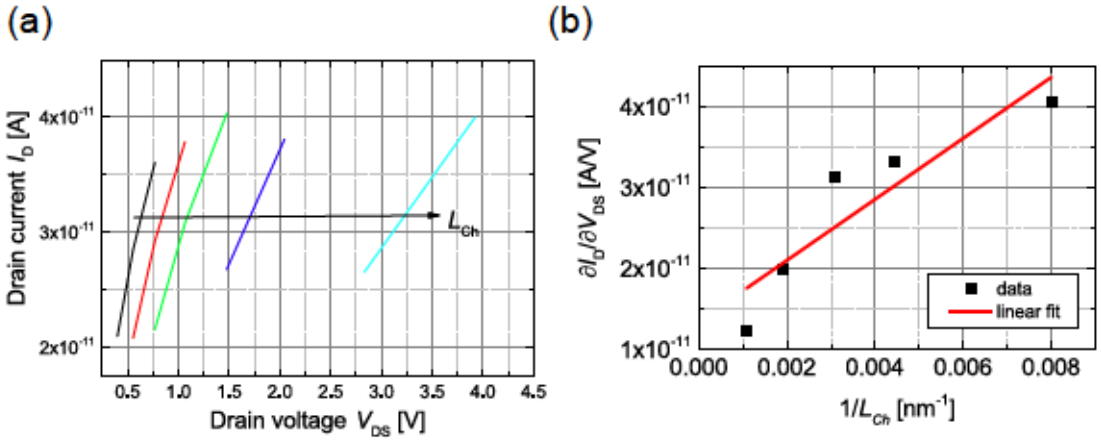


Figure 6.32.: (a) Simulated I_D versus V_{DS} for moderate V_{DS}, with colour coding as in figure 6.29. (b) Linear relationship between the gradient of the output characteristics in (a) and $1/L_{Ch}$.

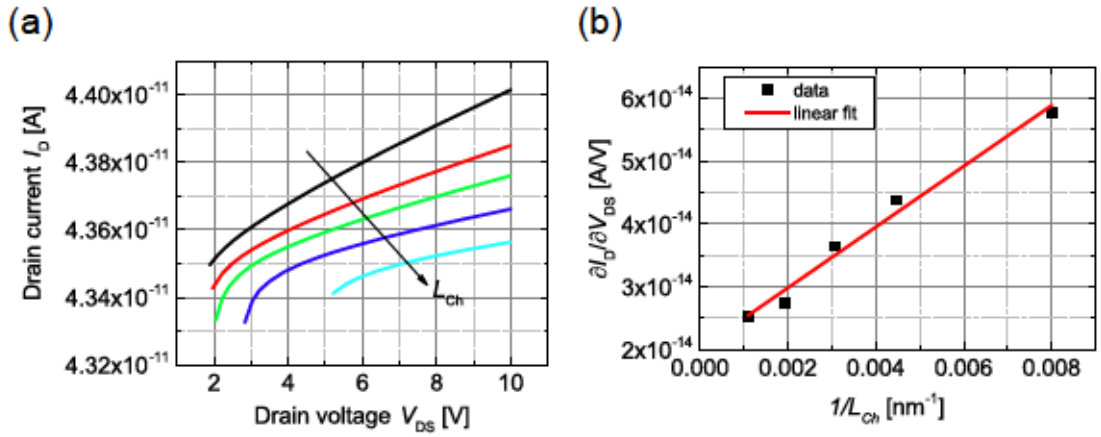


Figure 6.33.: (a) Simulated I_D versus V_{DS} for high V_{DS}, with colour coding as in figure 6.29. (b) Linear relationship between the gradient of the output characteristics in (a) and $1/L_{Ch}$.

the output characteristics, which is more pronounced for higher L_{Ch} due to the effectively lowered source-drain field. Equally, the linear relationships between the gradient of the output characteristics and L_{Ch} in the linear and saturation regimes are considerably more pronounced than for the case of the mobility variation discussed above.

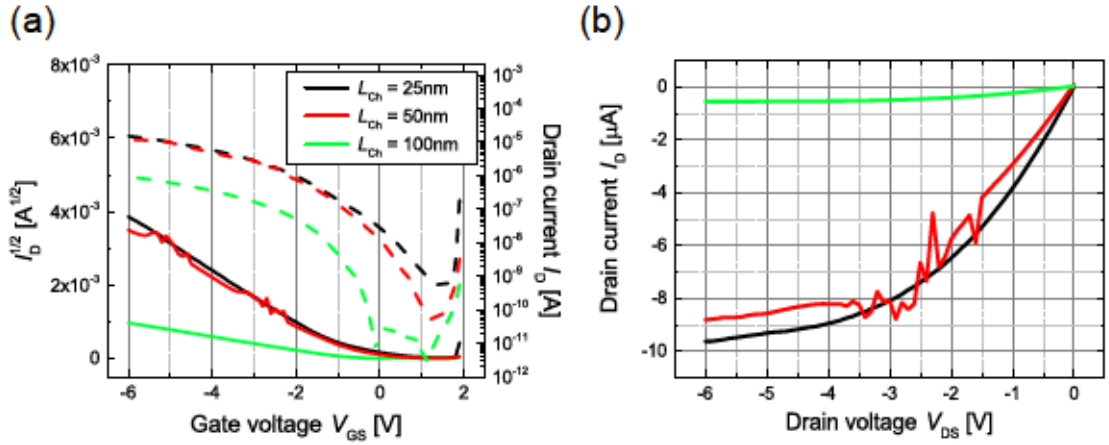


Figure 6.34.: Transfer (a) and output (b) characteristics of pentacene VOFETs built on the standard Si/Al_2O_3 substrates with varying thicknesses of the second pentacene layer. The applied drain voltage in (a) and the applied gate voltage in (b) are both -6 V. The thickness of the lower pentacene layer is 25 nm for all devices.

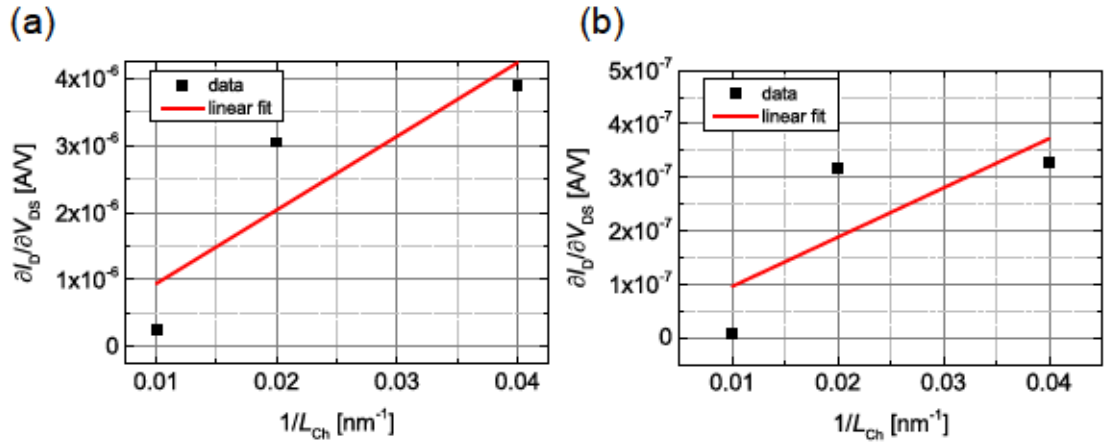


Figure 6.35.: Extracted gradients of the output characteristics shown in figure 6.34 (b) versus vertical channel layer thickness in the linear (a) and saturation (b) regimes of the output characteristics.

Figures 6.34 and 6.35 show attempts to replicate such behaviour experimentally for the standard pentacene VOFETs discussed before. An SCLC regime cannot be resolved here, most likely due to an overshadowing by other effects, such as an increased resistance in the accumulation layer. Since the sample with a channel layer thickness of 50 nm shows

an unstable transient, and repetitions of this experiment yielded similarly inconsistent results, it was difficult to replicate the linear trends expected from simulation (see figure 6.35). The more clearly resolved trends in the simulation, however, suggest that the VOFET architecture can be described by a formalism similar to the gradual channel approximation or indeed the gradual channel approximation itself.

6.5. SUMMARY

This chapter has introduced the simulation tool developed by the Weierstrass Institute for Applied Analysis and Stochastic to analyse the behaviour of an ideal VOFET geometry under various bias conditions. Combining a more thorough understanding of the VOFET's real geometry (obtained by SEM and TEM) with this simulation, a first rough understanding of the charge transport mechanisms in the VOFET was developed. Variations of the source insulator overlap in this simulation have indicated that an accumulation layer forms either at the gate dielectric or source insulator interface upon charge carrier injection (depending on the applied drain bias) and that its lateral extent depends on the size of the insulator overlap. This overlap thus strongly determines the electrical characteristics of the VOFET, not only by suppressing undesired leakage currents, but also by defining the active area of the device available for charge transport in the VOFET's linear regime. It was found that the saturation region of the VOFET is not affected by the exact size of the insulator overlap, as in the saturation regime, the channel is confined to the close proximity of the source electrode due to the strong drain field. Only the existence or absence of an insulator overlap affects the electrical characteristics in this regime by suppressing or allowing charge carrier emission from the vertical source edge. The simulation has further explained a trend observed experimentally in pentacene VOFETs: Connecting the VOFET's source and drain electrodes in reverse (source on top) leads to a noticeable decrease in On-State current while preserving or even increasing the On/Off ratio. The simulation has shown that this is due to effective charge carrier trapping at the insulator surface for reversed bias, where the degree of trapping depends on the exact geometry of the insulator overlap. In real devices, the beneficial effect on the On/Off ratio is diminished due to the non-ideal properties of this insulator.

These findings, particularly with regards to the vertical channel formation, were con-

firmed experimentally by measuring the light-emission from a VOLET stack. Further experimental work presented in this chapter has confirmed the mobility anisotropy of pentacene and demonstrated that the mobility can, to a certain extent, be tuned by controlling the deposition conditions of pentacene thin films. Lastly, combining the topic of mobility variations with the VOFET simulations has indicated SCLC behaviour of the ideal VOFET at very low drain bias, which was confirmed also by layer thickness variations in the vertical channel region. This layer thickness variation has further suggested a linear relationship between On-State current and the vertical channel layer thickness, as proposed by the gradual channel approximation for conventional OFETs. As these findings were partially backed by experimental data, it seems reasonable to assume that a behaviour at least similar to the gradual channel approximation can also be applied to VOFETs, particularly as there seems to be a similar formation of a charge accumulation layer which has a large effect on device performance.

7. DOPING CONCEPTS FOR VOFETS

In this chapter, the concept of doping will be introduced into the vertical transistor architecture, both as a means to improve the device performance and to gain an even better understanding of the operational principles governing this device geometry. Beginning with the simplest case of a doped semiconductor layer underneath the source electrode or in the vertical channel, the main part of the chapter will then focus on the introduction of selective contact doping as a proven method to enhance charge carrier injection. The effects of such selective doping will be studied further by use of the transmission line method introduced in the methods chapter, the results of which provide conclusive proof for the operational principles suggested in the previous chapter. Finally, the impact of these findings on the validity of the gradual channel approximation in VOFET devices will be discussed.

The previous chapter has introduced the idea that the VOFET geometry under investigation may in fact have an operation mechanism very similar to the conventional OFET, such that injection from the source electrode, accumulation at the gate dielectric interface and diffusion transport along this interface are indeed the limiting factors for VOFET performance. This hypothesis may be tested by introducing the concept of doping (see section 1.3) into this geometry. While doping has been successfully employed in conventional OFET structures in order to increase the conductivity of the lateral channel or enhance charge carrier injection into said channel, it has so far never been utilised for a VOFET structure or indeed any vertical organic transistor geometry, with the exception of the OPBT recently published by Kaschura *et al.* [305] and Klinger *et al.* [306].

This chapter aims to provide a systematic study of doping effects in the VOFET structure under investigation. Due to the adaptability of the layer-by-layer approach of producing these VOFETs, it is easily possible to selectively dope specific regions of the VOFET geometry and thus examine the impact that each of these regions has on the performance of the device. In this context, doping is thus used as an experimental tool to understand the importance of the individual parts of the VOFET and to verify the hypothesis of the previous chapter. If this hypothesis holds true, then selective doping should prove to be a powerful method to enhance VOFET performance.

7.1. DOPING OF THE BULK REGIONS

Doped organic semiconductors are typically used as transport layers in OLEDs and OSC [246], but have also been investigated for use in conventional OFETs. Olthof *et al.* and Hein *et al.* have demonstrated that a low concentrations of a suitable dopant in the channel region of an OFET can improve transistor performance by filling traps, particularly those deep traps often encountered at the gate dielectric interface [237, 307]. Hein *et al.* further showed that a p-doping effect also results in an increased bias stress stability of pentacene OFETs, which they attributed to a suppression of the proton migration mechanism [169]. A similar effect has also been observed by Oh *et al.* and can be produced either by doping of the entire semiconductor bulk or by application of a thin dopant layer to the channel region of the OFET [308]. Similarly, the application of such selective channel doping or bulk doping at low concentrations can improve the air-stability of n-type devices [308], while

a bulk p-doping at high concentrations has even been demonstrated to cause normally n-type C_{60} OFETs to operate as p-type transistors [65].

In the case of bulk doping, it is often observed that the field-effect mobility measured in the resultant OFETs increases for increasing doping concentration due to an efficient charge transfer process. In most cases, however, this increase in mobility goes hand in hand with a decrease in On/Off ratio, since the increase in conductivity also promotes leakage currents through the semiconductor bulk [252, 308–310]. For the special case of pentacene, bulk p-doping with MoO_3 has been demonstrated successfully in the past [252], as well as doping by larger organic molecules [247, 307]. However, as Kleemann *et al.* have demonstrated, the polycrystalline nature of pentacene may result in an actual decrease of mobility with increasing doping concentration due to a change of film morphology [247].

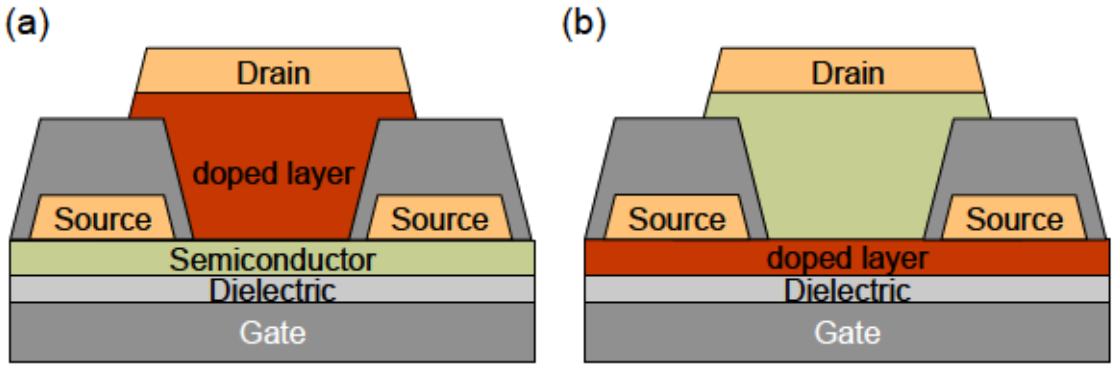


Figure 7.1.: Schematic representation of VOFETs with doped semiconductor layers: (a) a VOFET with an intrinsic semiconductor layer underneath the source and a doped vertical channel region and (b) a VOFET with an intrinsic vertical channel region and a doped semiconductor underneath the source. The dopant is indicated in red.

To investigate the effects of bulk doping on the pentacene VOFET's operation, either the bottom or top layer of pentacene are doped by F_6-TCNNQ with a doping concentration of 1.5 wt%, so as to avoid the disruption in film morphology observed by Kleemann *et al.* for higher doping concentrations. The device schematics for the doped devices are depicted in figure 7.1. These devices are manufactured in the usual manner (see chapter 4) on p-doped Si wafers with 30 nm of Al_2O_3 as gate dielectric, where either the first or second pentacene layer is co-evaporated with F_6-TCNNQ to produce the desired bulk doping. The transfer and output characteristics of these devices are shown in figure 7.2, with extracted performance parameters given in table 7.1.

As may be observed from figure 7.2 (a), bulk doping of the semiconductor layer un-

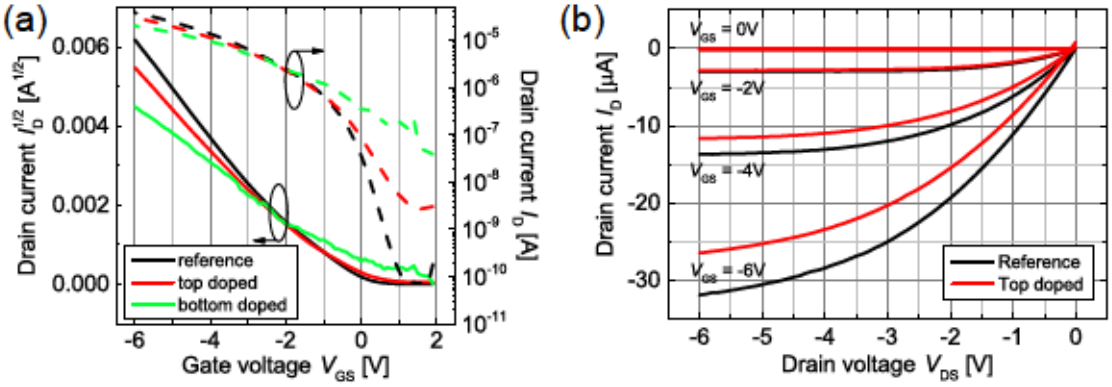


Figure 7.2.: Transfer characteristics (a) and output characteristics (b) of VOFETs with a doped vertical channel region (red) and a doped semiconductor underneath the source (green). A reference device without any doping is shown in black. Output characteristics of the bottom-doped device could not be obtained due to device instabilities and subsequent short-circuits in the measured devices. The applied drain voltage is V_{DS} = -6 V.

	V_{th} [V]	S [V/dec.]	g_m [µS]	On/Off ratio
reference	-0.96	0.39	12.45	7.9×10^5
top doped	-0.72	0.81	9.49	1.1×10^4
bottom doped	-0.19	1.57	5.37	156

Table 7.1.: VOFET parameters extracted for the devices shown in figure 7.2.

derneath the source electrode has a similar effect in the VOFET as reported previously for OFETs, namely the effect that the threshold voltage and On/Off ratio of the device decrease drastically, while the subthreshold swing increases noticeably. For the case of a conventional OFET geometry, both would be indicative of a strong p-doping effect in the transport layer, which results in higher conductivity and a reduction of contact resistance [252]. The fact that similar behaviour can be observed also in the VOFET geometry is a further strong indicator for the previously stated theory that the lateral charge transport near the gate dielectric interface plays a significant role in this device. Contrary to the bulk-doped OFETs reported in the literature, however, the transconductance of the VOFET decreases in comparison to the undoped reference device, which further promotes the decrease in On/Off ratio. The cause of this decrease in transconductance may be found in the decrease of pentacene mobility upon doping [247], as well as the processing conditions of the VOFET: As the doped layer underneath the source is subjected to two lithography steps and subsequent lift-offs, a reaction of the dopant with the fluorinated solvent used for these lift-offs may result in a further decrease of conductivity in the doped layer, e.g. due to washing out of the dopant. Unfortunately, all of the bottom-doped devices

investigated in this measurement series showed instabilities which lead to reproducible source-drain short-circuits when attempting to take output characteristics of these VOFETs. In light of the simulation results presented in the previous chapter, this may be due to the strong charge carrier accumulation near the source insulator for $|V_{DS}| > |V_{GS} - V_{th}|$.

Figure 7.2 also shows the transfer and output characteristics of a VOFET where the second layer of pentacene has been doped by 1.5 wt% of F_6-TCNNQ (compare figure 7.1 (a)). It is evident from these transfer characteristics and the parameters shown in table 7.1 that doping the upper bulk of the VOFET also has an effect on the device's operation. The effect, indeed, appears to be similar to that observed for the bottom-doped VOFET, albeit in a weakened manner. While lowering of the contact resistance at the source may be excluded in this case, the slight raise in conductivity of the upper pentacene layer still results in a lowered threshold voltage, while at the same time also providing higher leakage currents and thus a lower On/Off ratio. The increased subthreshold swing is here taken as an indicator for shallow trap states in the vertical channel due to ionised dopants. Although the conventional definition of the subthreshold swing in OFETs considers mainly trap states at the dielectric interface, the data obtained here suggests that the subthreshold swing may indeed be used as a general measure for trap states anywhere in a transistor geometry. Similar to the bottom-doped device, a decrease in transconductance is observed in comparison to the reference device. The fact that this decrease is smaller for the top-doped device strongly suggests that the same decrease in charge carrier mobility due to the disturbed morphology has less effect in this layer, i.e. that the transport path through the vertical channel is considerably shorter than the lateral transport underneath the source electrode, as predicted by the TEM measurements in the previous chapter (see section 6.1). It may further suggest that a reaction with the lift-off solvent HFE is another factor to be considered, as reactions with HFE should play a less pronounced role in the top doped layer (since this layer is subjected to only one lift-off procedure).

By comparing the two doped devices, one observes that doping of the bottom semiconductor layer has a greater effect on VOFET performance than doping of the top semiconductor layer. This indicates a limitation of the VOFET's performance by the lateral transport component, which in turn confirms that the lateral transport path is significantly longer than the vertical transport path, as suggested in the previous chapter.

7.2. SELECTIVE CONTACT DOPING[1]

The concept of contact doping, adopted from silicon technology [30], has been successfully employed in OFETs by inserting a thin injection layer between the metal contact and the organic semiconductor, which may be only a few nanometers thick and consists of a metal oxide (see e.g. [119]), self-assembled monolayer (SAM) [212], or organic compound [102, 120–123, 308, 311]. Insertion of a slightly thicker layer of the active semiconductor material, doped with a suitable p- or n-dopant, has also been reported as contact doping [76, 312, 313]. Both approaches are known to decrease contact resistance in bottom- as well as top-contact OFETs through various mechanisms [118] and are particularly important tools for counteracting the prominent contact effects often encountered in short-channel OFETs [102, 120, 126, 265] (see chapter 2). Such contact effects can also be observed in VOFETs [214, 217, 228, 230], as these devices typically have channel lengths on the order of a few micrometers or less, depending on the specific geometry. This contact limitation, while clearly observed in several VOFET devices so far [213, 214, 218, 227, 228, 230, 314], has not yet been addressed by specific contact engineering, as the basic proof of principle was often the aim of the respective publication. It stands to reason, however, that the concepts for contact doping established in lateral OFETs can directly be transferred to the VOFET architecture, especially in those cases where the device structure in the vicinity of the source contact resembles that of a lateral OFET [213, 214, 228, 230, 314]. Furthermore, the device architecture and fabrication process of certain vertical transistor geometries, such as the OPBT by Fischer *et al.* or the present VOFET geometry, allow for selective doping of the individual contacts without the need for additional structuring steps. Consequently, it is possible to separately investigate the effects of contact doping at the source and drain electrodes.

Presumably, the injection barrier for holes from Au into pentacene should be negligible because of the energy level alignment between the Au workfunction (approx. 5 eV) and the pentacene HOMO (approx. 5.1 eV). Basic metallisation effects [113] or impurities at the electrode-semiconductor interface, brought into the system e.g. during the photolithography process (see section 4.2.2), can already lead to the formation of a noticeable injection barrier, which manifests as a non-linear behaviour of the output characteristics of

[1] The text and figures in this section have mostly been published in ref. [268].

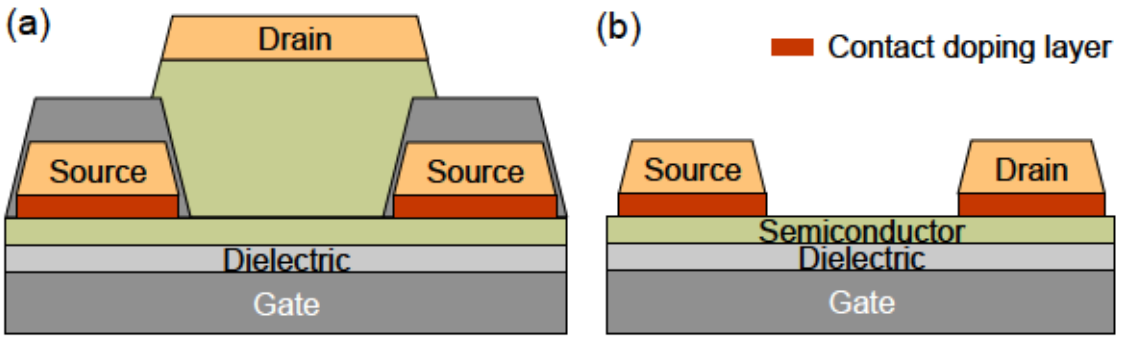


Figure 7.3.: Device structure for contact-doped VOFETs (a) and TLM OFETs (b), with contact doping layers indicated in red.

the VOFET at small drain voltages V_{DS}. Indeed, Watkins *et al.* reported a hole injection barrier from Au top contacts into pentacene as large as 1 eV [106], despite the seemingly well-matching energy levels of the pure materials.

To stabilise the interface and form a reproducible low injection barrier, two different contact doping approaches will be tested in the following sections: a thin layer of pure dopant underneath the VOFET source or drain electrode and a 10 nm-thick layer of pentacene, doped with varying concentrations of p-dopant in the same position. The fluorinated organic compounds $C_{60}F_{36}$ and F_6-TCNNQ are used as dopants, since both have demonstrated good doping properties for pentacene [29, 244]. The effect on contact resistance of each of these layers is further investigated by the transfer length method (TLM, see section 4.3) in the conventional staggered OFET geometry with the same material system and layer arrangement (see figure 7.3 (a) and (b) for a device schematic). This separate analysis is done in order to ensure that the TLM yields the correct results for the given materials and processing conditions, as it is unclear whether this analysis can be employed in a VOFET geometry. It is assumed, however, that the charge carrier injection mechanism in the OFET and VOFET is identical, so that the results of the TLM analysis in OFETs also describe the effects of contact doping in the VOFET accurately.

7.2.1. CONTACT DOPING BY A THIN INTER-LAYER OF $C_{60}F_{36}$

Firstly, the effects of contact doping by 2 nm-thin layers of pure $C_{60}F_{36}$ will be investigated. Such layers are inserted either between the source or the drain contact and the intrinsic semiconductor of the previously discussed p-type VOFET. The resultant transfer and output characteristics are shown in figure 7.4 and the extracted parameters for each device are

summarised in table 7.2.

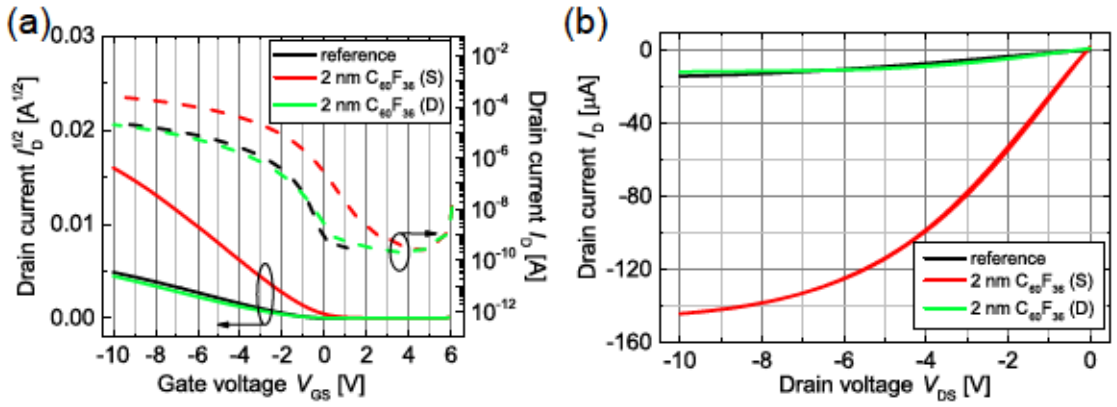


Figure 7.4.: Transfer characteristics at V_{DS} = -10 V (a) and output characteristics at V_{GS} = -10 V (b) of VOFETs with contact doping of 2 nm $C_{60}F_{36}$ underneath the source (red) and 2 nm $C_{60}F_{36}$ underneath the drain (green) respectively. A VOFET without contact doping is shown for reference (black). Extracted values are given in table 7.2. Previously published in ref. [268].

	V_{th} [V]	g_m [µS]	S [V/dec]	On/Off ratio
reference	-1.14	4.12	0.52	4.7×10^4
2 nm $C_{60}F_{36}$ (S)	-0.29	40.60	0.86	1.5×10^6
2 nm $C_{60}F_{36}$ (D)	-1.81	3.96	0.89	7.6×10^4

Table 7.2.: Extracted transistor parameters for devices displayed in figure 7.4.

It is immediately evident from this data that applying a thin layer of pure dopant as contact doping to the drain electrode primarily results in an increased subthreshold swing S (as defined by equ. 2.9), while having little effect on On-state current or On/Off ratio. In the present case, the additional traps, which lead to the increased subthreshold swing, are due to ionised dopant molecules near the extraction contact, rather than at the dielectric interface. The slight increase in On/Off ratio and threshold voltage (see table 7.2) can be explained by a lower leakage current due to charge carrier trapping near the drain. Evidently, the transconductance g_m is not improved upon doping the drain contact, as extraction of holes from pentacene into gold is very good already in the undoped system. Doping of the drain contact in pentacene VOFETs will thus not be considered any further.

Application of a thin layer of pure p-dopant between the source electrode and the semiconductor, on the other hand, significantly improves VOFET performance as indicated by figure 7.4. This effect is not simply due to a shift in threshold voltage (see table 7.2), but results from an actual reduction of contact resistance, as indicated by the fact that

also the transconductance g_m increases by one order of magnitude. A similar effect has previously been reported for short-channel OFETs (see e.g. ref. [102]), where also the saturation current of the OFET was improved slightly by the doping. The fact that this saturation current improvement is also more pronounced in the VOFET leads to the conclusion that the VOFET is more strongly injection-limited. The alternative explanation here would be that the conductivity of the accumulation layer in the saturation regime is improved as this, according to the data in the previous chapter, should be located near the source electrode and thus near the doped region. Due to the analogous findings of Ante *et al.* for OFETs, however, it is believed that this second explanation is less likely. The reasons for the significant improvement can be investigated in more detail by performing a TLM analysis on bottom-gate, top-contact OFETs. By using the same set of materials, substrate, geometry and fabrication process as for the VOFET devices (see figure 7.3 (b)), it is possible to transfer the results of such a TLM analysis directly to the VOFET geometry, as the injection behaviour in the OFET and VOFET devices must be identical. The extracted width-normalised contact resistance and transfer length are displayed in figure 7.5. A significant drop in contact resistance is observed upon doping and the V_{GS}-dependence of the contact resistance, typical for OFETs, is considerably weakened. The drop in contact resistance is further accompanied by an equally large reduction in the transfer length, with the latter becoming almost independent of V_{GS}.

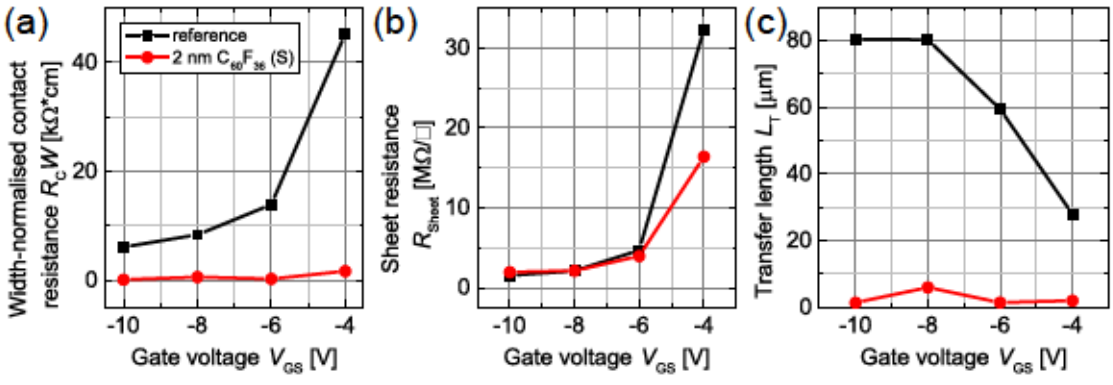


Figure 7.5.: Width-normalised contact resistance (a), sheet resistance (b) and transfer length (c) versus gate voltage, as extracted from the TLM analysis, for a contact-doped pentacene OFET with 2 nm $C_{60}F_{36}$ underneath the contacts (red) and a reference device (black). Published in ref. [268].

Due to the size of the dopant molecule and the morphology of the pentacene surface, the addition of nominally 2 nm of $C_{60}F_{36}$ (as measured by QCM) does not result in a closed

dopant layer, but rather in small islands of $C_{60}F_{36}$ accumulating on the surface of the pentacene film. This can be demonstrated via AFM imaging of a pentacene layer on the standard HMDS-treated Si substrate with 30 nm of Al_2O_3: Figure 7.6 shows tapping mode AFM images of a 30 nm-thick pentacene film on such a substrate, where a nominally 2 nm-thick layer of $C_{60}F_{36}$ has been deposited onto one half of the sample, while the other half of the substrate was covered. The increased surface roughness and larger number of small cluster features in figure 7.6 (b) points towards small clusters of the dopant forming on top of the pentacene layer, as has previously been observed for other dopants (see supporting information of ref. [102]).

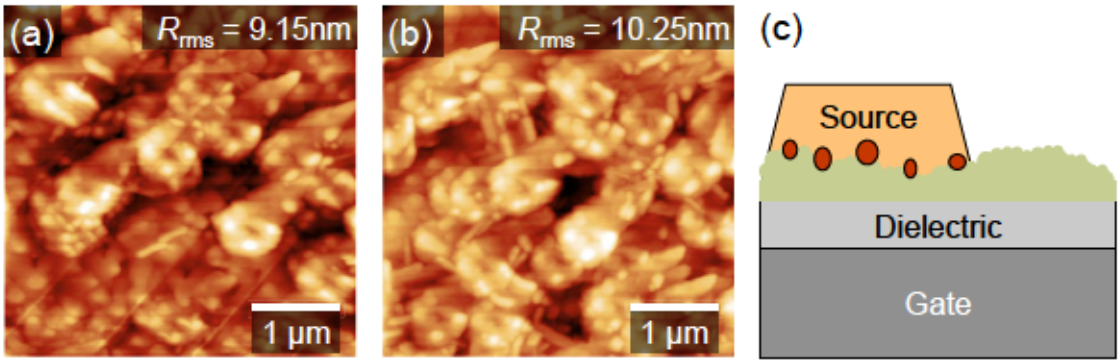


Figure 7.6.: Tapping mode AFM images of (a) 30 nm P5 and (b) 30 nm P5 with 2 nm $C_{60}F_{36}$ on top, both on silicon substrates coated with 30 nm Al_2O_3 and treated with HMDS. (c) Schematic representation of a more realistic source-semiconductor interface, with $C_{60}F_{36}$ clusters indicated in red. AFM images were published previously in the supporting information to ref. [268]

The presence of small $C_{60}F_{36}$ clusters is further evidenced by energy-dispersive X-ray spectroscopy (EDX), which has been performed on the source-drain overlap area of the contact-doped VOFETs[2]. As expected, the spectrum in the source region (figure 7.7 (a)) shows a weak, but visible peak for fluorine, while the channel region (figure 7.7 (b)) reveals no such peak. This is sufficient evidence that there are $C_{60}F_{36}$ molecules present underneath the source electrode. Note that the Au peak in figure 7.7 (a) stems from the Au source electrode, while the Si and Al peaks in both spectra originate from the underlying Si substrate with Al_2O_3 and – in the case of figure 7.7 (a) – from the SiO_2 above the source electrode.

It is to be expected that the size of the $C_{60}F_{36}$ molecule also largely prevents dopant diffusion into the underlying pentacene or even the channel region (compare channel

[2]EDX spectra were obtained by Petr Formánek (IPF Dresden) in a *Zeiss Ultra55* SEM, equipped with a *Bruker XFlash5060* EDX detector, at an acceleration voltage of 5 kV.

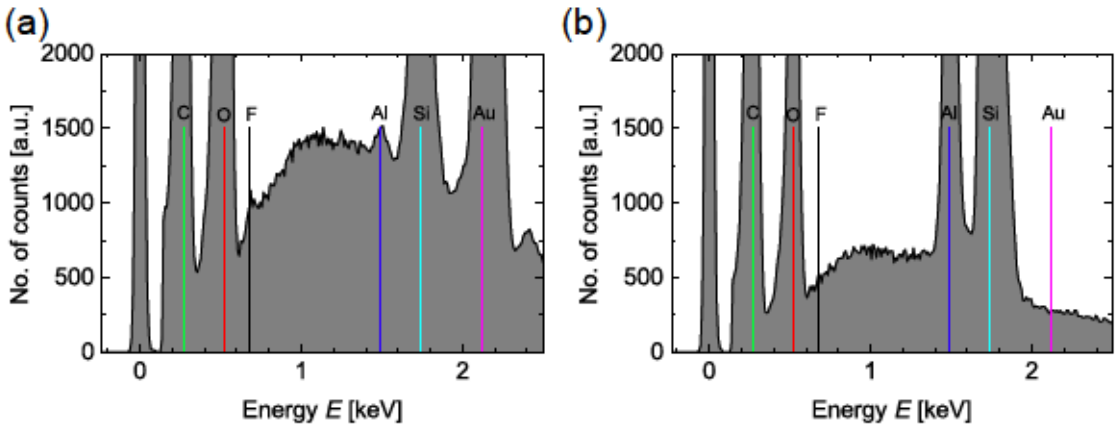


Figure 7.7.: EDX spectra of (a) the source contact area and (b) the channel area of a VOFET contact-doped with 2 nm $C_{60}F_{36}$ underneath the source. The expected K_α peaks for carbon (0.277 keV), oxygen (0.525 keV), fluorine (0.677 keV), aluminium (1.486 keV), silicon (1.739 keV) and gold (2.120 keV) are marked. Published previously in the supporting information to ref. [268]

resistances in figure 7.5). A certain degree of surface diffusion during processing is possible, but would not affect the channel volume either. Therefore, the resistivity of the bulk semiconductor between the source and the conductive channel should remain unchanged upon doping, so that the reduction in contact resistance must stem from an injection enhancement at the source contact. Indeed, the increased subthreshold swing of the doped device (see figure 7.4 and table 7.2) suggest that a large number of dopants have been ionised, i.e. that free charge carriers are available near the source-semiconductor interface. While it is at present not entirely known whether this doping process occurs via a direct charge transfer, as illustrated in figure 1.8, or by a matrix-dopant hybridisation [244], the obtained TLM and VOFET data suggests that a large number of free charge carriers are provided at the source-semiconductor interface upon doping. This results in a narrowing of the depletion region at the source contact and thus an effective narrowing of the Schottky barrier, so that injection from the source via tunnelling is enhanced. A further beneficial effect may be provided by the inherent roughness of the polycrystalline pentacene films: Some dopant clusters will naturally accumulate also within the thinner parts of the underlying pentacene film, a contact-doped region with narrower injection barrier may thus be located very near the gate dielectric interface. If several such regions are located close to the edge of the source contact, a large part of the transistor current may be injected from precisely these regions, which reduces the typical current crowding phenomenon (see section 2.3) and may thus explain the significant reduction in transfer

length observed for contact doping by such pure dopant layers.

7.2.2. COMPARISON TO THE STANDARD P-DOPANT F_6-TCNNQ

Another dopant which is frequently used to p-dope pentacene is F_6-TCNNQ. This material has a LUMO of 5.37 eV, but a lower activation energy and slightly higher doping efficiency in pentacene than $C_{60}F_{36}$ [29]. Supposedly, therefore, F_6-TCNNQ should produce even better contact doping results than $C_{60}F_{36}$. However, as figure 7.8 shows, the doping effect of a thin layer of F_6-TCNNQ is actually less pronounced, with the transconductance only improving by a factor of approximately 2.5 (as opposed to a factor of 10 for $C_{60}F_{36}$). This worse performance may be attributed to a partial damage of the F_6-TCNNQ during the subsequent processing steps of VOFET fabrication. Particularly the magnetron sputtering process used to deposit SiO_2 has the potential to introduce local heating of the organic layers due to high-energy ions hitting the sample surface, combined with exposure to UV radiation. It is believed that the higher glass transition temperature of $C_{60}F_{36}$ indicates better thermal stability of this molecule compared to F_6-TCNNQ, making the thin injection layer less likely to be destroyed when $C_{60}F_{36}$ is used instead of F_6-TCNNQ.

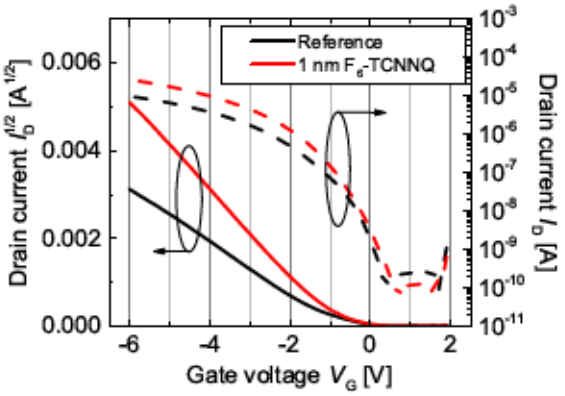


Figure 7.8.: Transfer characteristics of pentacene VOFETs without contact doping (black) and with a thin layer of 1 nm F_6-TCNNQ underneath the source (red). The applied drain voltage is V_{DS} = -6 V. The observed improvement in On-state current is only a factor of 2.5. Reproduced from the supporting information to ref. [268]

	V_{th} [V]	S [V/dec.]	g_m [µS]	On/Off ratio
reference	-0.86	0.37	3.02	1.1×10^5
1 nm F_6-TCNNQ (S)	-0.89	0.40	8.25	4.3×10^5

Table 7.3.: VOFET parameters extracted for the devices shown in figure 7.8.

A further advantage of $C_{60}F_{36}$ is its partial solubility in fluorinated solvents. Figure 7.9 shows the transfer characteristics of OFETs with 25 nm of pentacene and Au top contacts on Si wafers with 300 nm of SiO_2 as dielectric, which are measured directly after fabrication and again after 12 hours immersion in HFE, the stripper used during lift-off in the photolithography process (see section 4.2.2). For the central and right panel of figure 7.9, an unstructured, 2 nm-thin layer of $C_{60}F_{36}$ and F_6-TCNNQ respectively has been evaporated on top of the pentacene prior to photolithography and contact deposition.

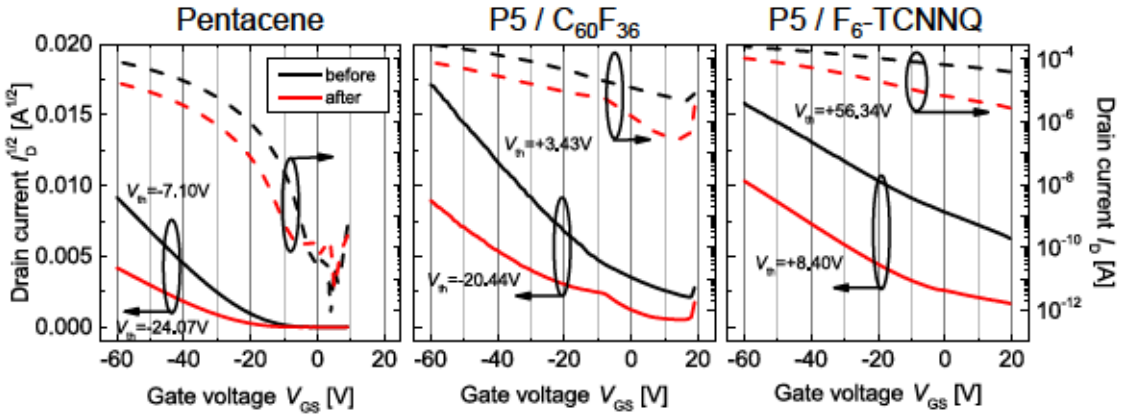


Figure 7.9.: Transfer characteristics of pentacene OFETs before (black) and after (red) immersion into HFE for 12 hours. From left to right: pure pentacene as active layer, pentacene with a 2 nm layer of $C_{60}F_{36}$ on top and pentacene with a 2 nm layer of F_6-TCNNQ on top. The applied drain voltage is V_{DS} = -60 V. Previously published in the supporting information to ref. [268]

The comparison of the transfer characteristics shows that a slight degradation is observed in each case simply due to the immersion of pentacene in HFE (see left panel of the figure). A layer of $C_{60}F_{36}$ evaporated onto the entire pentacene film prior to contact deposition results in a strong p-doping effect particularly in the upper regions of the pentacene film, thus providing contact doping, but also increasing the conductivity of the upper bulk region between the source and drain. Parasitic current consequently flows at the top of the pentacene layer, which cannot be controlled by the gate field and thus constitutes a large Off current. Upon immersion into HFE, some of this dopant seem to be washed out of this bulk region, while the dopant remains underneath the contacts. The threshold voltage thus shifts to the negative regime and a measurable On/Off ratio can be observed for this device. In the case of F_6-TCNNQ, the initial effect of the thin dopant layer is the same. In fact it is much stronger, suggesting better coverage by and possibly more diffusion of the smaller dopant molecules in combination with higher doping efficiency and conduction

through the dopant itself rather than the underlying pentacene. Upon immersion into HFE, the threshold voltage does shift, but still remains positive, while the On/Off ratio hardly improves. For VOFET fabrication, this means that a thin injection layer of $C_{60}F_{36}$ can actually be confined precisely to the source contact area, as dopants accidentally migrating out from underneath the Au electrode will be washed out by the subsequent photolithography processes. This, again, is in good agreement with the observed sheet resistances in figures 7.5 (b) and 7.11 (b).

7.2.3. CONTACT DOPING BY A MIXED LAYER

To examine the effect of a mixed layer doping approach, a set of VOFETs with varying concentrations of $C_{60}F_{36}$ in a 10 nm-thick pentacene injection layer is fabricated (analogous to the device structures shown in figure 7.3). The results of this experiment are shown in figure 7.10 and table 7.4. Here, a sample with an injection layer consisting of pentacene with 1 mol% of $C_{60}F_{36}$ in fact has a lower threshold voltage than the reference sample without doping (see table 7.4), yet the transconductance is noticeably lowered for this device, while increasing for higher doping concentrations.

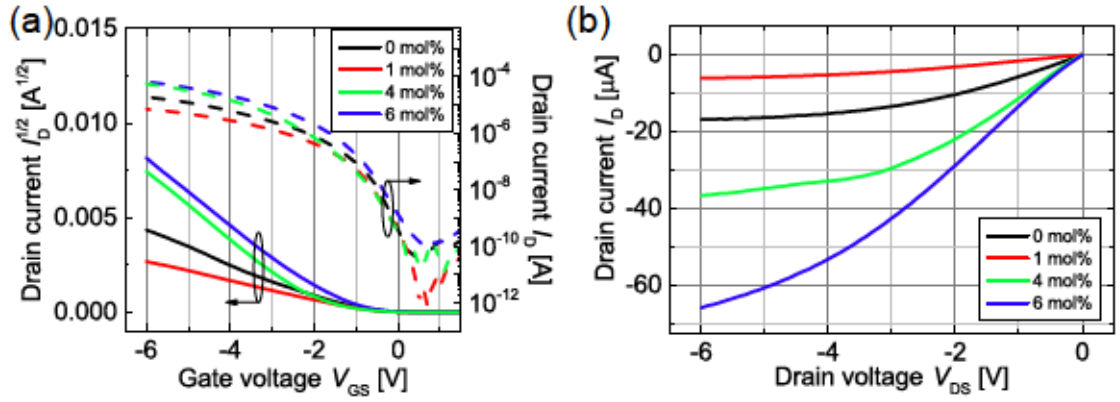


Figure 7.10.: Comparison of transfer characteristics at V_{DS} = -6 V (a) and output characteristics at V_{GS} = -6 V (b) between a reference VOFET (black) and VOFETs with a contact doping layer of 10 nm P5:$C_{60}F_{36}$ at doping ratios of 1 mol% (red), 4 mol% (green) and 6 mol% (blue). Extracted values are displayed in table 7.4. Previously published in ref. [268]

Once again, a TLM analysis of the equivalent OFETs yields an explanation for this phenomenon. As is visible from figure 7.11, the injection layer with 10 nm pentacene, doped by 1 mol% of $C_{60}F_{36}$, in fact increases the contact resistance and transfer length rather than reducing them. Only increasing the doping concentration to 4 mol% or higher

	V_{th} [V]	g_m [µS]	S [V/dec]	On/Off ratio
0 mol%	-1.37	6.22	0.34	4.75 x 10^5
1 mol%	-0.70	2.14	0.26	4.1 x 10^5
4 mol%	-1.88	20.88	0.39	4.9 x 10^5
6 mol%	-1.42	21.74	0.43	6.7 x 10^5

Table 7.4.: Extracted transistor parameters for devices displayed in figure 7.10.

results in a noticeable improvement in contact resistance and thus OFET and VOFET performance. At the same time, these more highly doped devices show an increased loss of saturation in comparison to the single layer doping approach (compare figures 7.4 and 7.10

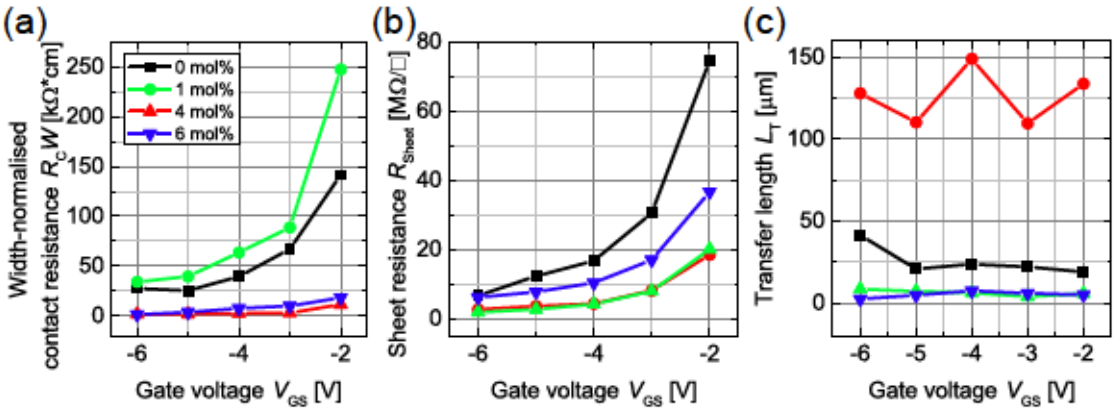


Figure 7.11.: Width-normalised contact resistance (a), sheet resistance (b) and transfer length (c) versus gate voltage, as extracted from the TLM analysis, for contact-doped pentacene OFETs with 10 nm P5:$C_{60}F_{36}$ underneath the contacts at doping concentrations of 1 mol% (red), 4 mol% (green) and 6 mol% (blue). A reference device without contact doping is shown as well (black). Previously published in ref. [268]

The effects of increasing doping concentration in a pentacene film can be investigated in a simple OFET geometry, as previously done for F_6-TCNNQ [247]. Performing conductivity and mobility measurements in such an OFET geometry reveals a clear trade-off between the increasing conductivity of a pentacene film, doped by $C_{60}F_{36}$, and the decreasing hole mobility. These two opposite effects are caused by a disruption of pentacene morphology and thus a decrease in grain size due to the dopant addition (see figures 7.12 and 7.13) and a simultaneous increase of trap filling and free charge carriers in the semiconductor due to the p-doping effect.

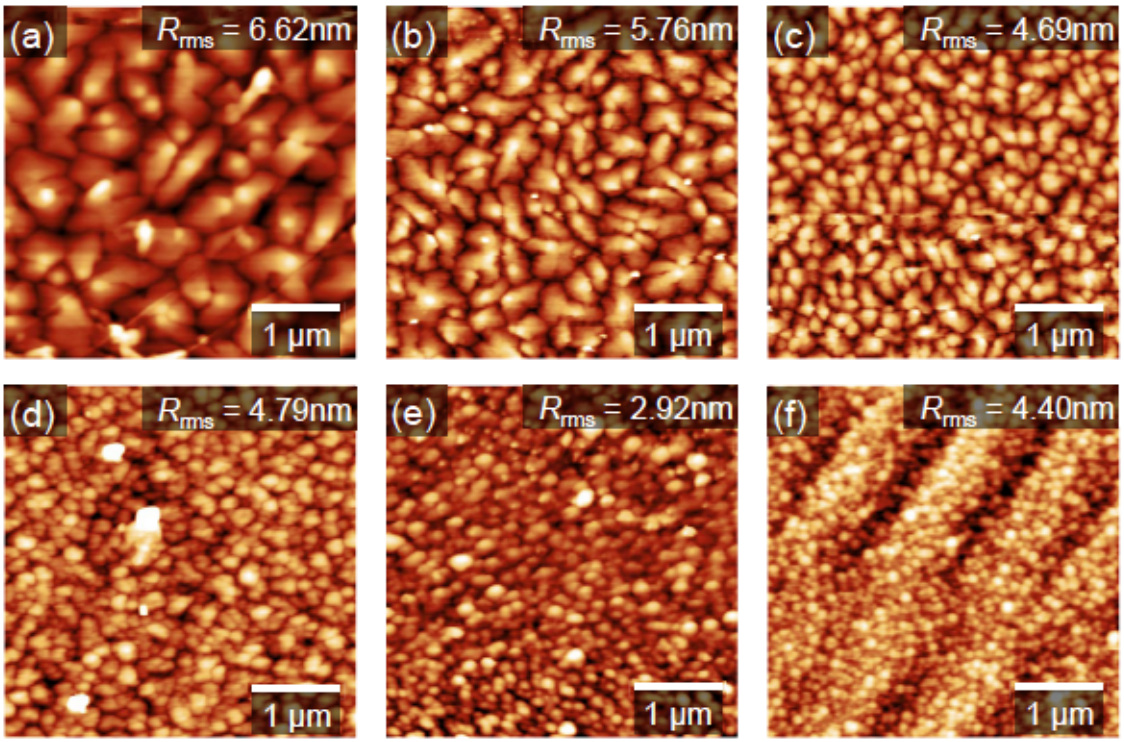


Figure 7.12.: Tapping mode AFM images of 30 nm P5:$C_{60}F_{36}$ in doping concentrations of 0 mol% (a), 1 mol% (b), 2 mol% (c), 4 mol% (d), 6 mol% (e) and 8 mol% (f) on silicon substrates coated with 30 nm Al_2O_3 and treated with HMDS. Previously published in part in ref. [268]

Consequently, a mixed layer of low doping concentration, inserted as injection layer between the VOFET's source contact and the semiconductor, provides a certain amount of trap filling and perhaps even free charge carriers. This may result in injection barrier narrowing, as discussed previously. At the same time, however, the mixed layer contributes an additional component to the bulk semiconductor resistance between the source and the conductive channel. This contribution is larger for mixed layers with low doping concentrations and may therefore outbalance the reduction in contact resistance due to barrier narrowing, as is the case for the 1 mol% layer investigated here. Increasing the doping concentration to 4 mol% or 6 mol% evidently results in a net positive effect, as the conductivity of these layers is higher (see figure 7.13), thus the contribution to the bulk resistance is decreased, while the increased doping concentration results in a larger number of free charge carriers (see subthreshold swing for these samples in table 7.4) and thus the expected barrier narrowing and improved injection. Comparing the characteristics of VOFETs employing different kinds of contact doping, it seems evident that from a processing point of view, application of a thin injection layer of pure dopant is the more

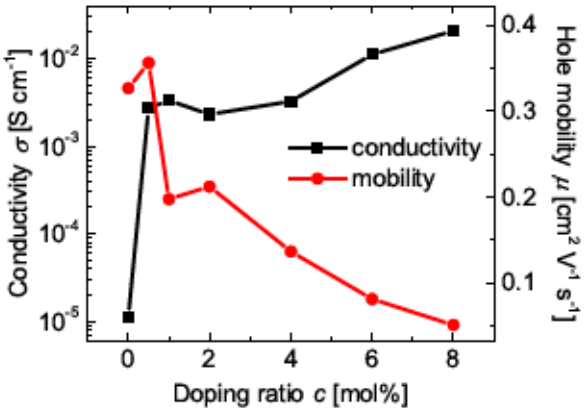


Figure 7.13.: Conductivity and mobility as functions of doping concentration, measured in an OFET geometry of 30 nm P5:$C_{60}F_{36}$ and 40 nm Au contacts on silicon substrates with 30 nm Al_2O_3 as gate dielectric, as previously done in ref. [247]. Published previously in ref. [268].

efficient choice, as it is easiest to implement and also provides the best On/Off ratio of all the devices presented here. The drawback of an increased subthreshold swing in this case may perhaps be tolerable for many applications as the significant reduction in threshold voltage still affords low driving voltages and thus makes these contact-doped VOFETs particularly interesting for applications with low power consumption.

7.3. IMPACT ON THE UNDERSTANDING OF VOFET OPERATION[3]

In the light of the results presented in the previous sections, it seems necessary to briefly re-visit the operational principles of the presented VOFET geometry: Firstly, the successful application of injection layers to the VOFET geometry proves conclusively that charge carriers are indeed injected from the bottom surface of the source contact, just as in a conventional top-contact OFET. The good On/Off ratios achieved through this mechanism further suggest that injection through the vertical edge of the source is suppressed, since it would otherwise constitute a considerable Off-state current (as observed e.g. by Stutzmann *et al.* and Parashkov *et al.* [213,214]). Examining the source-drain overlap region by scanning electron microscopy (SEM), one finds that the insulating layer of SiO_2, which is placed on top of the source electrode, does in fact have a considerable overlap into the vertical part of the channel and thus prevents injection from the edge of the source electrode. From the SEM image displayed in figure 6.1, it is possible to estimate this

[3]The figures and large parts of the text in this section have also been published in ref. [268]

overlap as L_{ins} = 3.2 µm. A charge carrier emitted from the source electrode into the underlying semiconductor must consequently move at least this distance L_{ins} inside the lower semiconductor layer before it is able to enter the vertical channel and be collected by the drain electrode. This, however, is only true for charge carriers emitted directly at the edge of the source contact. The majority of carriers, however, will be injected from within an area $A = WL_T$ of the source electrode's bottom surface, where W is the width of the source contact and L_T is the transfer length as defined before. The average distance travelled by any charge carrier inside the VOFET is thus gate-voltage-dependent and may be used as an effective channel length for the VOFET, given as

$$L_{eff}\left(V_{GS}\right) = L_{Ch} + L_T\left(V_{GS}\right) + L_{ins} \tag{7.1}$$

where L_{Ch} is the length of the vertical channel, $L_T(V_G)$ the gate-voltage-dependent transfer length (as extracted from TLM analysis) and L_{ins} the overlap length of the source insulator over the vertical edge of the source contact. Within the crowded current model [115], the transfer length can also be expressed as

$$L_T = \sqrt{\frac{r_C}{W r_{Ch}}} \tag{7.2}$$

where r_C and r_{Ch} are the contact and channel resistivities respectively. Using

$$r_{Ch} = \frac{1}{W C_{diel} \mu \left(V_{GS} - V_{th}\right)} \tag{7.3}$$

for the channel resistivity, the gate-voltage-dependent transfer length becomes

$$L_T\left(V_{GS}\right) = \sqrt{r_C C_{diel} \mu \left(V_{GS} - V_{th}\right)} \tag{7.4}$$

Using the effective mobility μ and the contact resistivity r_C as fit parameters, one may fit this equation to the TLM data presented in the previous sections. This is done in the lower sections of figure 7.14 (a) and (b) (red line). It is further possible to insert this expression into equ. 7.1, so as to obtain an expression for the effective channel length of the VOFET which is gate-voltage-dependent.

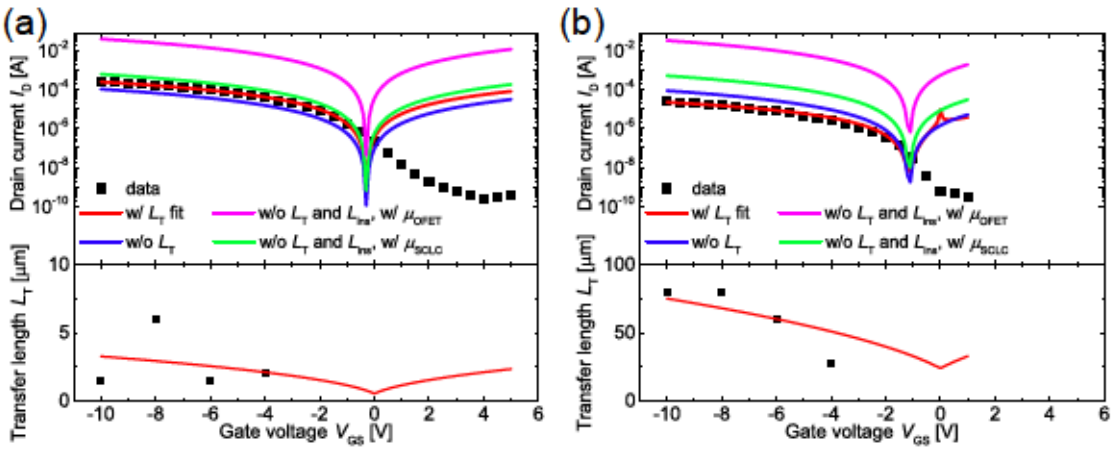


Figure 7.14.: Measured (black squares) and simulated (lines) transfer characteristics of the contact-doped (a) and reference (b) devices presented in figure 7.5. The simulated curves are produced by using equ. 2.3 and 7.1 and assuming L_{Ch} = 50 nm and L_{ins} = 3.2 µm. Fit parameters for the red lines are μ = 0.27 $cm^2V^{-1}s^{-1}$ and r_C = 1.66 x 10^{-5} Ωm for the contact-doped device in (a) and μ = 0.34 $cm^2V^{-1}s^{-1}$ and r_C = 6.46 x 10^{-3} Ωm for the reference device in (b). Other fits are obtained by excluding either the transfer length (blue) or both transfer length and insulator overlap (green and purple) from equ. 7.1. The green line is then obtained using a lower vertical mobility for pentacene, as suggested by ref. [231], while the purple line represents the transfer characteristics of a VOFET with the previously used values for µ and only considering the vertical channel length. Reprinted from ref. [268]

In the devices presented here, it has been demonstrated that $L_{Ch} \ll L_T + L_{ins}$ and so charge transport in the VOFET may be dominated by the horizontal diffusion transport near the gate dielectric interface, rather than drift transport in the vertical channel. If this is the case, then it should be possible to model the characteristics of a VOFET by the standard expression derived from the gradual channel approximation, i.e. by equ. 2.3. Using equ. 7.1 and 7.4 for the channel length in this expression, the transfer characteristics of the reference device and contact-doped device discussed in section 7.2.1 have been fitted. A least-squares algorithm has been employed to determine the best fit parameters for μ and r_C and the results of this fit are displayed in the upper sections of figure 7.14 (a) and (b) (red lines). It is indeed found that the use of the effective channel length describes the observed transfer characteristics of these devices well, provided that one assumes an effective mobility in the pentacene layers which is lower than the typically measured field-effect mobilities. The best fit parameters are μ = 0.27 $cm^2V^{-1}s^{-1}$ and r_C = 1.66 x 10^{-5} Ωm for the contact-doped device (figure 7.14 (a)) and μ = 0.34 $cm^2V^{-1}s^{-1}$ and r_C = 6.46 x 10^{-3} Ωm for the reference device (figure 7.14 (b)). The mobilities obtained from the

fit are in good agreement with those determined from the transfer characteristics of the equivalent OFETs during TLM. Figure 7.14 (a) and (b) further show fit lines obtained by removing the L_T term from equ. 7.4 (blue line) or by excluding both L_T and L_{ins} and using only L_{Ch} as effective VOFET channel length. In the latter case, fits have been attempted both with the previously used values for μ (purple line) and with a lower mobility for transport through the vertical channel as approximated in a previous publication [231] (green line). From these latter fits it is immediately obvious that inclusion of both L_T and L_{ins} into the effective channel length is vital in order to model the correct transfer characteristics. This, in turn, is conclusive proof that the vertical transport, even when considering the lowered mobility for pentacene in this direction [231], is not the limiting factor in this VOFET geometry. In the case of a proper fit with voltage-dependent L_T and L_{ins} as measured by SEM, the fitting functions for both devices show inaccuracies at lower V_{GS} due to the lack of L_T data obtained in this region. Nevertheless, this simple simulation illustrates that it is indeed possible to describe the present VOFET geometry as an OFET, i.e. by the gradual channel approximation, if one takes into account the insulator overlap and transfer length as limiting parameters for the effective transistor channel length. While the VOFET structure, at first glance, differs significantly from the conventional OFET, the present condition of $L_{Ch} \ll L_T + L_{ins}$ may be used to interpret the VOFET as a short-channel OFET with $L \approx L_T + L_{ins}$, where transport through the vertical channel may simply be included as a larger contact resistance at the drain electrode. Together with the experimental data presented in the previous sections, this now represents a much more complete understanding of the VOFET geometry discussed here, as well as similar geometries published previously by other groups [213, 214, 218, 221, 227, 228, 314]. It is evident from the data that while many groups working on such VOFET geometries claim to have reduced their device's channel length to 1 µm or less, a truly accurate description of a VOFET can only be given if the total transport path, including especially the transfer length of the source contact and (in geometries similar to the present one) the insulator overlap, is known. Devices such as those of Stutzmann *et al.* [214] and Parashkov *et al.* [213, 314], which emit charge carriers from a vertical source edge, are free of horizontal transport contributions and consequently limited in the On-state by a space-charge current through the vertical channel, which results in the observed loss of saturation (a typical short-channel effect). Onsets of such behaviour can also be observed for sufficiently doped VOFETs of

the type presented here, as illustrated by the output characteristics in figures 7.4 (b) and 7.10 (b). The fact that figure 7.10 (b) shows a more pronounced lack of saturation than figure 7.4 (b) may now also be explained in the context of equ. 7.1: By inserting a 10 nm thick layer of doped pentacene only underneath the source contacts, the geometry of the devices may have changed in such a way that the shadowing effect during SiO_2 deposition is altered, resulting in a shorter source insulator overlap in these devices. The absence of short-channel effects in a VOFET geometry may point towards a comparatively long transport path and in such cases it certainly seems necessary to address the question of transfer length and other horizontal transport contributions to the total transport path of the device. In this respect, the addition of pentacene layers only underneath the source contacts may perhaps be exploited as an additional tool to reduce L_{ins}.

7.4. SUMMARY

The impact of introducing doping into a VOFET geometry has been discussed in this chapter, both in the context of improving VOFET performance and as a tool to gain a better understanding of the operational principles of this geometry. Bulk doping of individual semiconductor layers within the VOFET geometry has indicated a dominance of lateral transport near the gate dielectric interface of the VOFET, with a weaker contribution from transport through the vertical channel. This is in accordance with the simulation data by the WIAS presented in the previous chapter.

The use of selective contact doping has further clarified the VOFET operation mechanism. As suggested also by the WIAS simulations, doping in the vicinity of the drain electrode has very little effect on the device performance. A highly doped interface at the source electrode, however, results in a significant increase in performance. Using data from a TLM analysis of equivalent OFET geometries, this improvement is attributed to a reduction in transfer length and thus a reduction in the total lateral charge transport path inside the VOFET. Finally, fitting a gate-voltage-dependent expression for the transfer length to the obtained TLM data and using this fit, together with the insulator overlap length determined in the previous chapter, as an effective channel length afforded to fit the VOFET's transfer characteristics to the standard gradual channel approximation. Through this fit it can be demonstrated that a good approximation to the operational mechanism of the present

VOFET geometry is in fact a standard OFET with the fitted effective channel length and a slightly higher contact resistance at the drain electrode (in order to account for the short vertical channel, see figure 7.15).

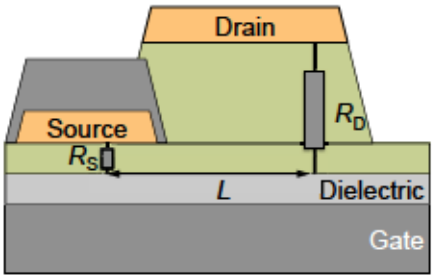


Figure 7.15.: Schematic representation of the VOFET structure with proposed channel length and contact resistances indicated.

One may conclude from this that a key factor in improving VOFET performance is the reduction of the device's transfer length via efficient contact doping, as well as the reduction of the insulator overlap length by a more precise structuring and deposition mechanism. Only when these two characteristic lengths are reduced to the order of 1 µm or less will the present VOFET (and indeed any vertical transistor of a similar geometry) truly be a short-channel device and approaching a working mechanism which is dominated by transport through the vertical channel.

8. VERTICAL ORGANIC INVERSION TRANSISTORS

In this last results chapter, the potential of inversion mode operation in the vertical architecture is discussed. Using the information gathered in the previous chapters, a concept for inversion mode operation in VOFETs is established and tested in a suitable material system. The chapter concludes with a systematic study of how VOFET parameters can be controlled by inversion mode operation.

The previous chapters have given conclusive proof of the operational principle of the VOFET architecture. It has been established that the device operates in an accumulation mode almost identical to that of the conventional OFET and that it is therefore possible to improve the VOFET's On-state current by the same methods as applied in conventional OFETs, namely control of the transfer length, semiconductor morphology and quality of the gate dielectric interface. So far, however, the control of other parameters, in particular the threshold voltage, has not been discussed.

While in some applications, the requirement for the threshold voltage is merely that it should be as low as possible so as to reduce power consumption, logic circuits based on a CMOS-like approach may require a more precise control of this parameter. In most of the vertical transistor architectures presented to date, fine-tuning of specific parameters is difficult. Contact doping may be easy to implement into some of these devices, yet this only provides a limited control over the threshold voltage (see chapter 7). Fine-tuning of this parameter is hardly possible in these devices, as is also the case for most conventional OFETs. While in CMOS, MOSFETs operate in inversion mode and the threshold voltage control is thus achieved by control over the substrate's doping concentration [30], Brondijk *et al*. have argued that transfer of this concept into organic electronics is not possible, as the inefficient injection of minority charge carriers in OFETs prevents inversion mode operation [315]. In particular, they showed that electron currents cannot be obtained in p-doped P3HT OFETs, thus excluding the formation of an inversion layer in the OFET channel region.

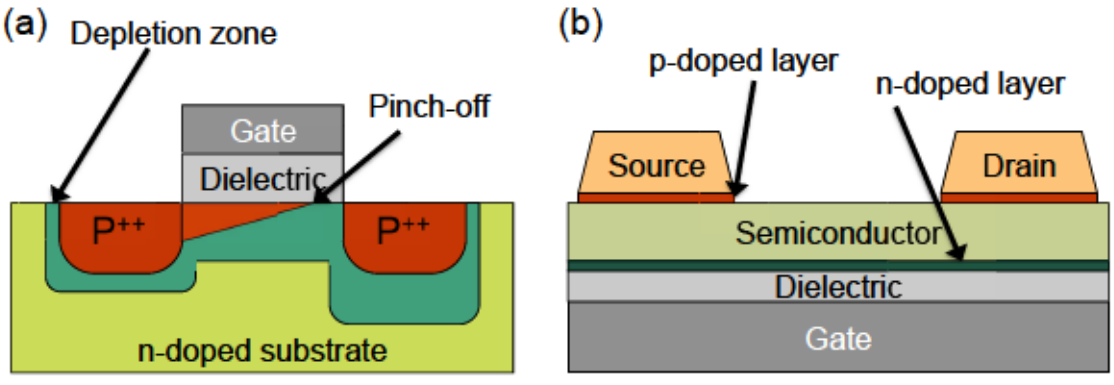


Figure 8.1.: (a) Schematic representation of a classical inversion mode MOSFET in saturation. The depletion zone around the p-doped contacts is indicated in dark green, the pinched-off p-channel is indicated in red. (b) Equivalent inversion OFET published by Lüssem *et al*.

In 2013, Lüssem *et al.* proposed an alternative approach to realising inversion mode operation in organic semiconductors [100, 312]: Rather than doping the entire semiconductor bulk, as attempted by Brondijk *et al.* [315], Lüssem *et al.* [312] and later Liu *et al.* [100] doped only the channel region close to the dielectric interface. By placing an n-doped channel layer in a normally p-type pentacene OFET and adding injection layers of p-doped pentacene, they were able to create sufficient injection of holes into the n-doped layer at the dielectric interface, thus inverting specifically this layer, while keeping the semiconductor bulk unchanged. Without a detailed characterisation e.g. by AFM, it is arguable whether the 6 nm-thin n-doped pentacene layer used by Lüssem *et al.* does indeed form a closed layer[1], thus necessitating inversion for the observed hole current, or whether the observed hole current is actually transported through a network of intrinsic pentacene grains located in-between n-doped regions (which might then merely act as additional trap sites). Nevertheless, both Lüssem *et al.* and Liu *et al.* were able to control the threshold voltage of their OFETs by adjusting the doping concentration of this n-doped layer, thus facilitating the effect ultimately desired in inversion mode operation.

Applying this concept to the present VOFET geometry should therefore facilitate similar control over the threshold voltage and, when combined with the improvements detailed in previous chapters, may offer the potential for true high-performance devices with finely tuneable parameters.

8.1. DISCUSSION OF SUITABLE MATERIAL SYSTEMS

When following the concept of Lüssem *et al.* to realise an organic inversion transistor, the right choice of organic materials is crucial: An organic semiconductor must be found which can easily be incorporated into the VOFET manufacturing process, has good transport properties in its intrinsic state and can be doped with both n-type and p-type dopants, so as to allow for the formation of an inversion layer and the efficient injection of minority carriers into this layer. Both Lüssem *et al.* and Liu *et al.* chose pentacene (P5) as the active material of a p-type inversion OFET, as it can easily be p-doped, e.g. by F_6-TCNNQ [244], and n-doped, e.g. by $W_2(hpp)_4$ [244] and provides good hole transport parameters in its intrinsic state.

The system P5:$W_2(hpp)_4$, however, is not air-stable, as the very shallow HOMO of

[1] It is generally believed that pentacene only begins to form closed layers well above 10 nm.

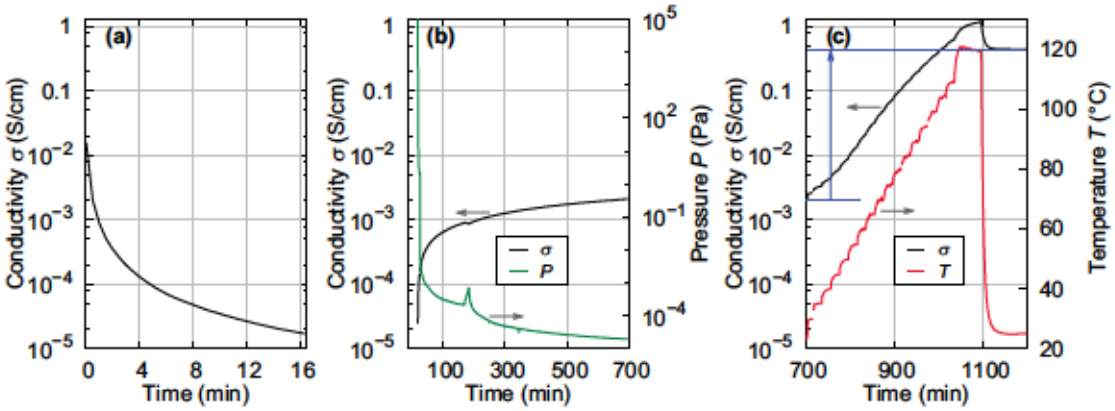


Figure 8.2.: Conductivity of a C_{60} thin film n-doped by 4 wt% of $W_2(hpp)_4$ (MR = 0.033). (a) Freshly prepared and annealed at 120°C (t = 0, measured at 25°C) followed by an air exposure for 16 min, (b) during re-evacuating to high-vacuum conditions, and (c) during final annealing in vacuum. Reprinted from ref. [316] with permission of Wiley.

$W_2(hpp)_4$ (see table 4.2) causes an immediate decomposition of most dopant molecules upon exposure to oxygen. This system is therefore unsuitable to be used in a VOFET geometry, as the doping effect of an n-doped inversion layer near the dielectric interface would be lost during the photolithography processes. Investigations of Tietze *et al.* on the system C_{60}:$W_2(hpp)_4$ suggest that a certain amount of dopant can survive this initial degradation process through self-passivation, so that a doping effect can be recovered through annealing (see Figure 8.2). According to Tietze *et al.*, the number of dopant molecules which are protected via this mechanism can be increased by choosing matrix materials with deeper-lying energy levels. A potential replacement for pentacene may therefore be DNTT (see table 4.1), whose transport properties are similar to those of pentacene, but which has considerably deeper HOMO level due to its non-linear structure [236]. However, with an optical gap of 3.0 eV (compared to 1.8 eV for pentacene), it is questionable whether DNTT can be doped by $W_2(hpp)_4$ and whether this system is then indeed more air-stable.

Figure 8.3 shows the conductivity of a 20 nm-thick film of DNTT:$W_2(hpp)_4$ as a function of time. The initial conductivity is determined to be approximately 3×10^{-6} Scm^{-1} in vacuum. After transferring the sample to a nitrogen glovebox at t = 800 s the measured conductivity begins to decrease. At t = 1950 s the sample is exposed to air. At this stage, the conductivity decays below the resolution limit of the SMU used for the measurement. This data clearly indicates that while DNTT itself is more air-stable than pentacene due to its

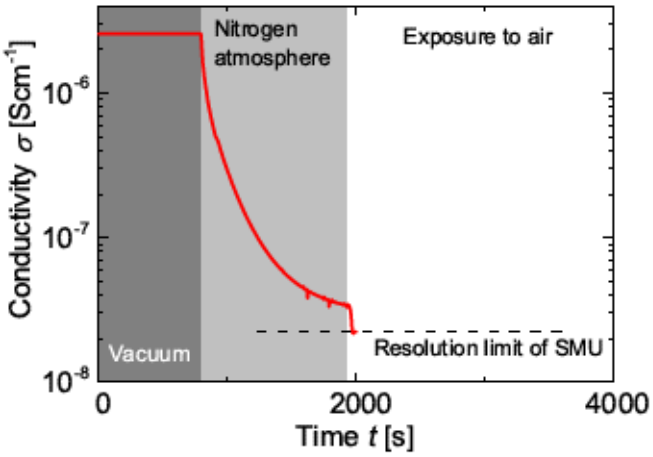


Figure 8.3.: Conductivity versus time for a sample of 20 nm DNTT, doped with 7 wt% of $W_2(hpp)_4$. Measurement by Martin Schwarze and Olka Kaveh, IAPP.

deeper HOMO, this deep HOMO does not provide sufficient protection for the dopant as proposed by Tietze *et al.*, neither is the initial charge transfer process from $W_2(hpp)_4$ into the DNTT LUMO efficient enough to provide good electron conductivity even in vacuum. The system DNTT:$W_2(hpp)_4$ is consequently not suitable as an n-doped inversion layer for inversion VOFETs.

Instead, we use a matrix material which has already been demonstrated to provide well-functioning VOFETs: the Buckminster fullerene C_{60}, which has been used by Kleemann *et al.* to demonstrate n-type VOFETs with good performance and which is highly compatible with the photolithography process [90, 230]. The spherical shape of this molecule and the resultant stacking properties ensure that the layer morphology of doped C_{60} differs very little from the intrinsic material, which is beneficial for the VOFET geometry. Furthermore, C_{60} forms closed layers already at a layer thickness of approximately 5 nm, as indicated by conductivity measurements [317]. Recently, Lee *et al.* have shown that it is possible to achieve efficient hole transport in the normally n-type C_{60} by doping with high concentrations of MoO_3 [65]. It should therefore be possible to fabricate n-type VOFETs with a strongly p-doped inversion layer, where the active material is C_{60}. If one wants to employ contact doping to enhance injection, one does of course face the same issue of finding air-stable n-dopants again. However, as demonstrated by Kleemann *et al.*, the injection of electrons from Au electrodes into intrinsic C_{60} is efficient enough to provide high currents in VOFETs and may therefore not need to be improved further in order to realise inversion VOFETs. Furthermore, the work function of Au is approximately half-way

between the LUMO and HOMO of C_{60} (Au work function = 5.1 eV, C_{60} HOMO = 6.4 eV, C_{60} LUMO = 4.0 eV [239, 318, 319]), the injection barriers for both carrier types are thus roughly comparable, allowing for both (majority and minority) carrier types to be injected into the doped inversion layer.

8.2. REALISING INVERSION VOFETS[2]

Following the discussion in the previous section and also the approach of Lüssem *et al.*, it is vital to check that accumulation of both minority and majority carriers is indeed possible within the doped inversion layer. It must further be investigated how this accumulation behaviour depends on the thickness and doping concentration of the p-doped inversion layer. This is done by building a series of m-i-s stacks (see chapter 4) with the same layer stack as the inversion VOFET will have underneath the source electrode, i.e. in the region relevant for accumulation. This m-i-s stack, along with the proposed inversion VOFET, is shown in figure 8.4.

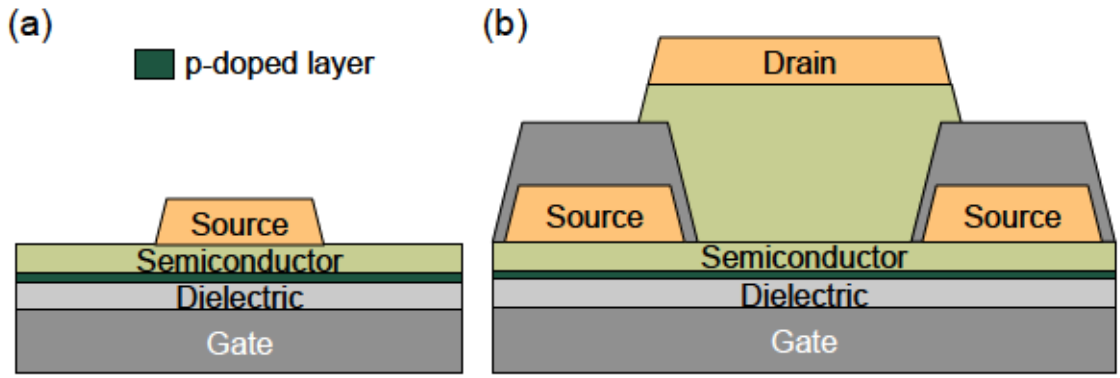


Figure 8.4.: (a) Device schematic of the m-i-s capacitors used for *CV* characterisation and (b) device schematic of the VOFET with a p-doped layer for inversion operation.

The m-i-s capacitors are built on the same substrate type as the VOFETs (see chapter 4), so as to ensure comparability between the two device types. All m-i-s capacitor samples are prepared in a single run in the single-chamber UHV tool and are never exposed to air prior to characterisation to prevent additional p-doping by oxygen. This is also particularly necessary as the energy levels of MoO_3 shift upon contact with air. The original levels can be recovered via annealing [65].

In order to characterise the accumulation behaviour inside the inversion layer, capacit-

[2]Most of the text and figures presented in this section have previously been published in ref. [320].

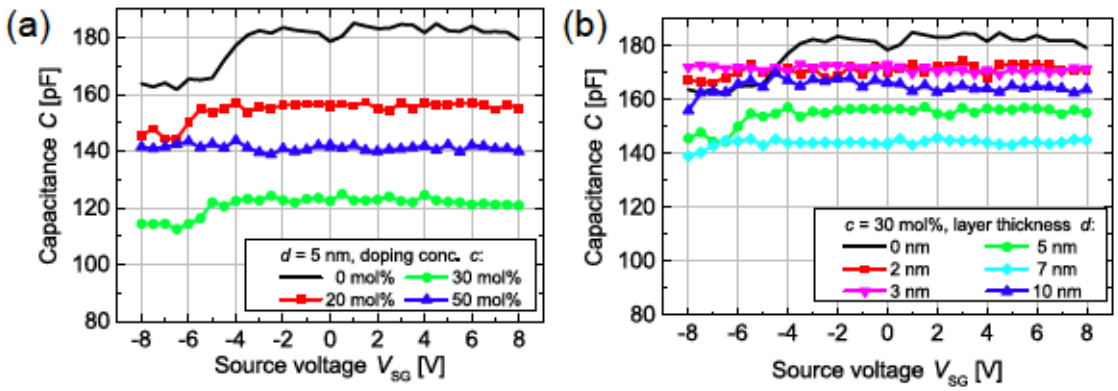


Figure 8.5.: *CV* characteristics of (a) samples with a fixed doping layer thickness of 5 nm and varying doping concentrations of MoO_3 and (b) samples with a fixed MoO_3 concentration of 30 mol% and varying doping layer thicknesses (with constant d_{tot}). The turn-over point between majority carrier accumulation and depletion is marked as a dashed line and a reference device without a p-doped C_{60} layer is shown as a black line.

ance-voltage spectroscopy (*CV*) is performed on the m-i-s capacitor stacks. *CV* curves are obtained at a frequency of 100 kHz and an amplitude of 50 mV. The DC voltage is applied to the injecting top contact, while the substrate, i.e. the back contact, is kept at ground potential. The total capacitance per unit area of the m-i-s stack can be approximated as

$$\frac{1}{C} = \frac{1}{C_{\text{diel}}} + \frac{1}{C_{\text{inv}}} + \frac{1}{C_{\text{semi}}} = \frac{d_{\text{diel}}}{\varepsilon_0 \varepsilon_{\text{diel}}} + \frac{V_{\text{SG}}}{nd} + \frac{d_{\text{tot}} - d}{\varepsilon_0 \varepsilon_{\text{semi}}}, \tag{8.1}$$

where C_{diel}, C_{inv} and C_{semi} are the capacitances per unit area of the gate oxide, inversion layer and intrinsic semiconductor layer. n is the charge carrier density inside the inversion layer, which depends on the doping concentration, d_{diel}, d and d_{tot} are the oxide, inversion layer and total semiconductor thicknesses and all other variables have the same meaning as in the previous chapters. As can be observed in figure 8.5, the total capacitance varies noticeably between the individual samples. This is attributed to the variation predicted by equation 8.1 as well as variations in d_{tot} due to dopant addition and small variations in device area due to processing conditions.

The application of a positive voltage to the injecting contact results in the accumulation of holes at the interface between the p-doped C_{60} and the underlying Al_2O_3. This hole accumulation effect is observed not only for the samples with a p-doped layer, but to a certain extent also for the undoped reference sample, shown in black. This can be attributed to the processing conditions in the chamber: All samples were prepared in a

single run and even though a wedging tool covered the reference samples during MoO_3 deposition, a slight MoO_3 contamination of the reference samples is possible. Applying a negative voltage to the injection contact instead accumulates electrons at the dielectric interface, i.e. the inversion regime is reached. The turn-over point between these regimes is marked in figure 8.5 as a dashed line for each sample. As the doping concentration or doping layer thickness at the dielectric interface is increased in a controlled manner, one observes a shift of the turn-over points, as typically observed for MOSFETs with a high-frequency test signal [30]. The inversion regime can only partly be resolved in highly doped samples due to experimental limitations: The characterisation tool used for the *CV* measurements is limited to the voltage regime investigated here and low frequency measurements (which typically show a clear accumulation of minority carriers in inversion MOSFETs) could not produce reliable results due to the noise level in and around the glovebox. n-type contact doping would normally be employed in such a case to enhance the injection of minority charge carriers and thus make the inversion regime more visible. This, however, would once again necessitate an air-stable n-dopant for C_{60}[3]. Nevertheless, figure 8.5 clearly shows that it is possible to deplete the p-doped inversion layer and thus allow for accumulation of minority electrons instead. Inversion mode operation of an n-type C_{60} VOFET with a p-doped layer at the gate dielectric interface should thus be possible.

To investigate the effects of the inversion layer on the working VOFET, the transfer characteristics of a series of VOFETs with the same p-doped layers are measured in the saturation regime. The transistor threshold voltage V_{th}, which can be extracted from these transfer characteristics, is expected to depend on the density of activated dopants $N_A(c)$ and on the doping layer thickness d according to

$$V_{th} = V_{FB} + \frac{eN_A(c)d}{C_{diel}}, \tag{8.2}$$

where V_{FB} is the transistor flatband voltage, c the doping concentration and e the elementary charge [312]. To obtain transfer characteristics, V_{GS} is swept in the same way as for the *CV* measurement.

[3]The annealing step suggested by Tietze *et al.* is an option only if the total air exposure time during VOFET processing is reduced. The procedure followed in this thesis involves two processing steps in air which each last up to 90 min. Figure 8.2 (a) suggests a strong decay of conductivity for such times, which may not be fully recovered by annealing.

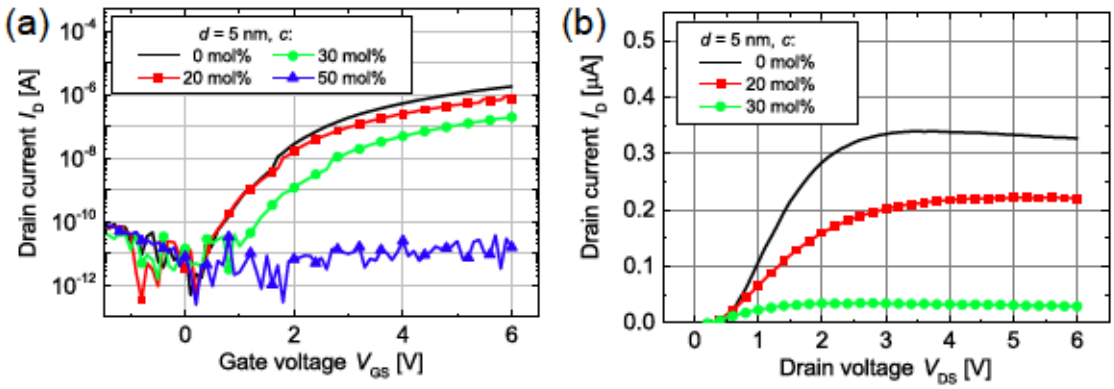


Figure 8.6.: (a) Transfer curves of VOFETs with a fixed doping layer thickness of 5 nm and varying doping concentrations of MoO_3. The applied V_{DS} is 6 V. (b) Output characteristics of the same VOFETs at V_{GS} = 6 V. Reference devices without a p-doped C_{60} layer are shown as black lines in both cases.

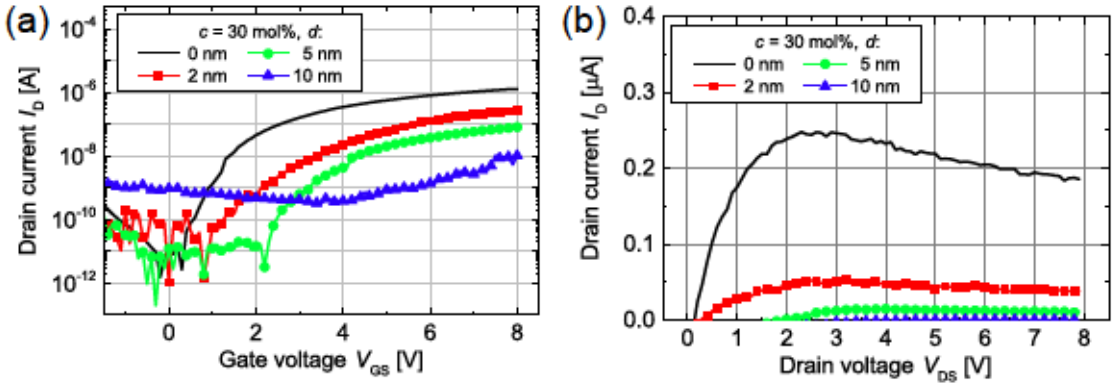


Figure 8.7.: (a) Transfer curves of VOFETs with a fixed doping layer concentration of 30 mol% and varying doping layer thickness. The applied V_{DS} is 8 V. (b) Output characteristics of the same VOFETs at V_{GS} = 8 V. Reference devices without a p-doped C_{60} layer are shown as black lines in both cases.

Figures 8.6 (a) and 8.8 (a) show a controlled threshold voltage shift with increasing doping concentration in the inversion channel. This same effect was previously demonstrated by Lüssem *et al.* [312]. It may be noted that the V_{th} determined from the transfer characteristics is not identical to the turn-over point marked in the *CV* curves in figure 8.5. This is attributed to differences in processing conditions and slight variations in dielectric thickness (substrates for m-i-s stacks were produced at IAPP, those for VOFETs at IHM, see chapter 4). It can further be shown that the threshold voltage is shifted towards higher voltages by an increased thickness of the doped layer, as suggested by equ. 8.2. As can be observed from figures 8.7 (a) and 8.8 (a), a change in layer thickness does in fact produce a more systematic threshold voltage shift than a change in doping concentration, as layer thickness is more easily controlled than doping concentration, at least for the system

C_{60}:MoO_3 in the evaporation system used for the deposition of the inversion layer[4]. The output characteristics of this set of transistors additionally exhibit a certain degree of bias stress in the form of decreasing I_D in the saturation regime (see figure 8.7 (b)), an effect which is less pronounced in figure 8.6 (b). This bias stress is most likely related to proton migration or OH^- ion diffusion into the dielectric, as suggested by Colléaux *et al.* [321].

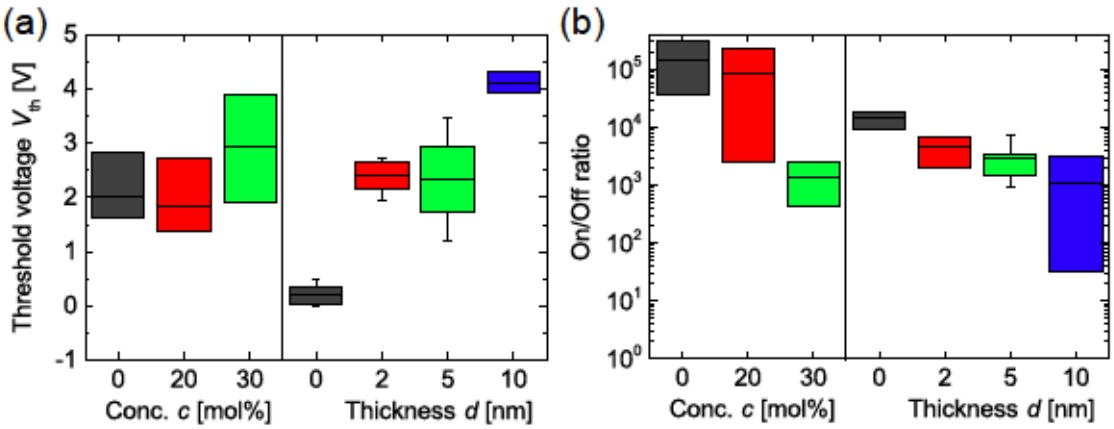


Figure 8.8.: Threshold voltage (a) and On/Off ratio (b) as a function of doping concentration and doping layer thickness for at least three devices per sample. Box areas represent the interval of 25% to 75% of the data distribution, whiskers denote the maximum and minimum values of the distribution. The horizontal black lines within the boxes represent the mean value of the distribution. For a concentration of 50 mol%, no data could be extracted, as is visible from the lack of switching behaviour in figure 8.6.

These findings, together with the *CV* measurements, are further proof that the V_{th} shift is due to an increased number of holes near the gate dielectric interface, resulting from the p-doping effect of MoO_3 in C_{60}. Once the holes are depleted from the doped layer, it is possible to accumulate electrons at the gate dielectric interface in the same way as in the reference VOFET. The precise voltage at which this turn-over happens, i.e. V_{th}, is determined by the amount of holes in the p-doped layer. A fit to equ. 8.2 (see figure 8.9) yields transistor flatband voltages V_{FB} of 1.85 V and 0.82 V for the concentration and thickness variation series respectively. In the case of the thickness variation with c = 30 mol%, a density of activated dopants $N_A(c) \approx 5 \times 10^{18}$ cm^{-3} is given by the fit, which is similar to the density of activated dopants found by Lüssem *et al.* [312] and suggests a very low doping efficiency of MoO_3 in C_{60} (< 1%), as indicated by Lee *et al.* [65].

[4]The maximum deposition rate achievable for C_{60} in this system was 0.2 Å/s, thus the evaporation rate of MoO_3 had to be kept very low in order to realise low doping concentrations. Precise control at such low values was difficult, as the evaporation of MoO_3 powder from a metal evaporator (see chapter 4) is much less homogeneous and controlled than e.g. that of C_{60} from a crucible.

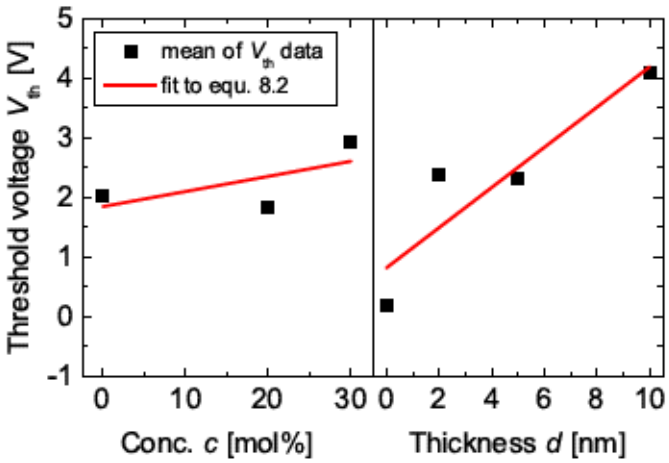


Figure 8.9.: Mean values for V_{th} as a function of doping layer concentration c and doping layer thickness d (black squares), extracted from figure 8.8 (a). Fits for this data to equ. 8.2 are indicated as red lines.

The presented data suggests another benefit of the inversion operation which has not been demonstrated before: The p-doping layer at the gate dielectric interface allows for control of the Off-state current. As is visible in figure 8.6, a comparably small MoO_3 concentration of 20 mol% does not yet affect the threshold voltage much, but results in the presence of a small amount of holes near the gate dielectric interface. This leads to carrier recombination with the electrons leaking out of the source electrode in the transistor's Off-state. This effect reduces the Off -state current while having only a slight effect on the On-state current. If combined with an efficient dopant inter-layer as injection booster at the source (see chapter 7), this effect could provide a useful tool to enhance the On/Off ratio in VOFETs. As higher MoO_3 concentrations introduce more holes into the p-doped layer, however, there are no longer sufficient amounts of electrons from the source-drain leakage current to recombine with, thus the holes themselves now form a considerable leakage current in the Off-state of the transistor, as can be seen particularly well for an MoO_3 concentration of 50 mol% or a doped layer thickness of 10 nm.

8.3. SUMMARY

The results presented in this chapter show that vertical organic field-effect transistors can be improved by using the inversion operation concept. Variations in the doping concentration or layer thickness of a p-doped layer in an n-type VOFET can control the threshold voltage and Off-state current of the device, with the layer thickness variation

producing a particularly controlled shift of these parameters. Indeed, the reduction of leakage currents, and thus the potential for improving the On/Off ratio, is an especially interesting feature of this operation, since leakage currents are an issue often faced in short-channel devices. If an air-stable n-dopant can be incorporated into the VOFET manufacturing process or processing can be done without contact to air in the future, the combination of inversion mode operation and the inter-layer contact doping presented in the previous chapter will present a set of powerful tools for the controlled manipulation and improvement of VOFETs, facilitating threshold voltage control and very high On/Off ratios. These two mechanisms combined can provide the boost for VOFETs required to make them true short-channel high-performance devices suitable for a wide range of electronics applications.

9. CONCLUSION AND OUTLOOK

The results obtained in the previous chapters will briefly be summarised once again in this last chapter of the thesis and their applicability to other VOFET geometries will be discussed. Lastly, suggestions will be made concerning the further improvement and better understanding of the VOFET.

9.1. CONCLUSION

The aim of this thesis was to provide a better understanding of the operational principles of the VOFET geometry published by Kleemann *et al.* in 2013 [230]. This has been accomplished through a combination of experiments and simulations: A closer look at the manufacturing process of the VOFET in chapter 5 has highlighted the importance of the source insulator, its geometry, material quality and deposition technique. The latter has been found to be of particular importance, as an invasive deposition technique, such as sputtering or thermal ALD at high T, may damage the underlying organic semiconductor layer and thus lead to a decrease in transistor performance. The drift-diffusion simulations presented in chapter 6 confirmed the influence of this lower semiconductor layer on charge transport. Here, it was shown that charge carriers are emitted primarily from the bottom surface of the source electrode and thus diffuse through the lower semiconductor layer before forming a conductive vertical channel directly at the source insulator edge. The length of this diffusion path is determined by the length of the source insulator's overlap over the vertical edge of the source electrode, which was measured with electron microscopy to be approximately 3 µm - 4 µm for real VOFETs. The simulation showed that this long overlap is indeed beneficial for the On/Off ratio of the device, while a complete lack of source insulator overlap results in a low On/Off ratio due to additional and uncontrolled charge carrier emission from the vertical edge of the source also in the Off-state.

Through variations of the gate and drain bias, the linear ($|V_{DS}| < |V_{GS} - V_{th}|$) and saturation ($|V_{DS}| > |V_{GS} - V_{th}|$) regimes were also investigated in the simulation. It was found that the linear regime of the VOFET is almost identical to that of a conventional OFET, as charge carriers here accumulate at the gate dielectric interface before drifting through the vertical channel. Furthermore, the total current in this regime was found to be limited by the volume of semiconductor available for charge transport in the vertical channel, which leads to a saturation of the transfer characteristics at high V_{GS} where the entire semiconductor bulk is used to conduct the vertical channel current. By varying the length of the vertical channel as well as the mobility in this regime, this effect was resolved in more detail: For $|V_{DS}| \ll |V_{GS} - V_{th}|$, the VOFET is limited by an SCLC regime in the vertical channel due to the high carrier density and efficient diffusion transport in

the bottom semiconductor layer. At $|V_{DS}| < |V_{GS} - V_{th}|$, this resolves into the well-known linear OFET regime. The saturation regime with $|V_{DS}| > |V_{GS} - V_{th}|$ differs slightly from the standard OFET behaviour. Although the gradual channel approximation seems to hold, the simulation showed that charge accumulation in this regime actually takes place not at the dielectric interface, but at the source insulator interface. In this regime, the vertical channel also becomes narrower again due to the stronger pull of the drain field. This behaviour in the simulations was also replicated in experiments by using light-emitting VOFETs to visualise the vertical channel formation.

With this much more thorough understanding of the VOFET's operational principles it was possible to manipulate the VOFET performance in a controlled manner: By applying the concept of molecular doping to the VOFET's different regions, it was possible to show that selective doping of the source contact can significantly improve charge carrier injection and thus the VOFET's On-state current and On/Off ratio, while doping of the drain electrode has no effect. It was thus concluded that in contrast to the simulation, where ohmic injection has been assumed, the real VOFET is strongly injection-limited due to the Schottky barrier between the source (made of Au) and the semiconductor (pentacene). By doping the direct vicinity of the metal, the depletion region at the Schottky barrier is reduced and injection via tunnelling thus enhanced. Doping the bulk of the organic semiconductor underneath or above the source electrode, however, has a less beneficial effect, most likely due to the large number of ionised dopant molecules and resultant scattering and shielding effects. Selective doping of the vicinity of the gate dielectric interface, on the other hand, allowed to demonstrate for the first time inversion mode operation in a vertical organic transistor by accumulating minority charge carriers in this doped region. By varying either the doping concentration or the doping layer thickness in such inversion mode VOFETs, it is possible to control the threshold voltage and - to a certain extent - also the Off-state current of the device. From these experimental findings it was finally concluded that the present VOFET geometry resembles a conventional OFET in enough aspects to use the gradual channel approximation as a first, rough approximation also for the VOFET.

The ideas which have been put forward in this thesis regarding the detailed operational principle of the VOFET geometry are most likely also applicable to the closely related step-edge devices (see chapter 3) and therefore provide a general framework to describe

the operation of any vertical organic transistor architecture which relies on a similar field-effect concept. It is believed that this framework may even be applied to OSBTs, as these devices mostly resemble a VOFET without a bottom semiconductor layer and without a source insulator overlap. Working from this analogy, the vertical channel in such OSBTs should also form directly at the vertical source edge, as predicted for a VOFET without an insulator overlap (see chapter 6). This assumption, however, contradicts the findings of Ben-Sasson *et al.*, whose simulations of the OSBT suggest a channel formation in the centre of the source openings rather than the edges [203]. A direct comparison of Ben-Sasson's work with an OSBT simulated by the WIAS team may therefore be necessary in order to clarify this matter. For devices which rely on a charge carrier injection and transport mechanism similar to those of the VOFET, the selective doping approaches discussed above provide a complete set of tools to tailor the parameters of the vertical device to specific applications.

9.2. OUTLOOK

While this thesis provides a qualitative understanding of the VOFET's operational principles, as well as methods to improve the VOFET's operation, it has also become clear that the current VOFET design, as suggested by Kleemann *et al.* [230], is still limited not only by charge carrier injection from the source electrode, but also by the lateral diffusion transport underneath the source electrode. This makes the device rather more similar to a conventional OFET than would be desirable for short-channel devices and high-performance applications. Future work on the VOFET must therefore address this limitation by optimising first of all the source insulator overlap geometry. A considerably shorter overlap of less than 1 µm may perhaps be achieved with a more careful undercut control during photolithography (perhaps with a different fluorinated resist), different deposition conditions or even an insulating SAM. The latter, in particular, might also be combined with organic insulators such as TTC to decrease the amount of invasive processing procedures and to thus increase the yield during processing, as well as the quality of the finished devices.

From a material science and engineering point of view, much material and geometry optimisation can of course be done in order to tailor the VOFET to market applications such as AMOLED control matrices or integrated circuits for e.g. RFID tags, where high

On/Off ratios, high switching frequencies and good threshold voltage control are desirable. From a physicist's point of view, however, another interesting topic may be the more detailed investigation of the VOFET's saturation regime, where at high drain bias the accumulation layer underneath the source should move up towards the source insulator interface according to the simulation data. Since no clear indicator for this effect has so far been found in experiments, a more thorough investigation of this matter could yield interesting results, as well as a better understanding of the comparability of simulation and real device.

In order to gain a better understanding of the VOFET's suitability for different applications, a full high-frequency characterisation as well as bias stress tests will also become necessary. Such measurements will certainly open up new routes for device optimisation, as well as posing new and interesting questions. Especially the topic of bias stress is generally not very well understood, also for the case of OFETs, and may be more complex in vertical architectures. Here, too, doping may prove to be a useful tool, as it has previously been shown to counteract the effects of bias stress in OFETs [307].

If such improvements are made, then vertical organic field-effect transistors may not only surpass conventional OFETs in terms of initial performance and stability, but may also become truly successful organic electronics devices capable of bridging the gap between low-cost manufacturing and high performance.

APPENDIX

A. XRD SPECTRA OF PENTACENE FILMS

X-ray diffraction (XRD) measurements were performed by Dr. Lutz Wilde of the Center Nanoelectronic Technologies (Fraunhofer Institute for Photonic Microsystems, Dresden). For these measurements, pentacene films of varying thickness were deposited on Si substrates with 30 nm Al_2O_3 at different deposition rates. The XRD spectra obtained by Dr. Lutz Wilde were analysed by Dr. Chris Elschner (formerly of IAPP).

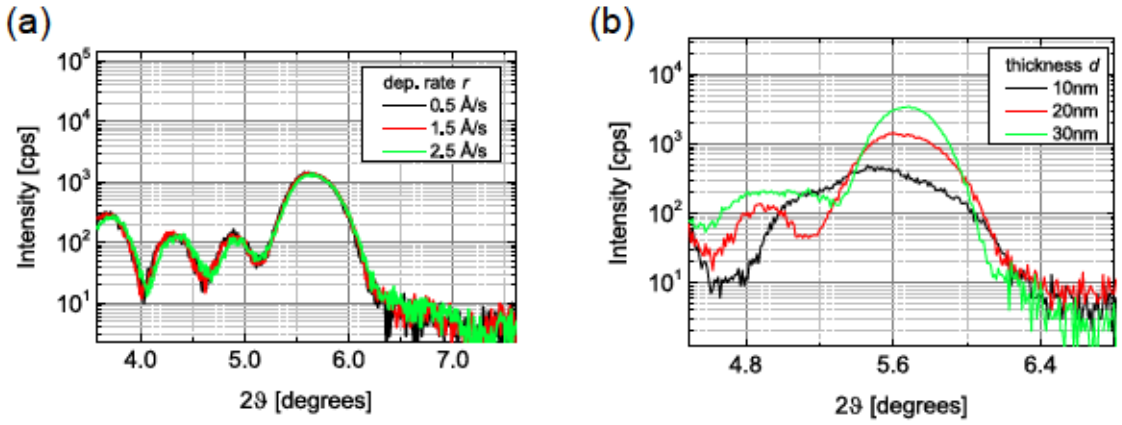


Figure A.1.: XRD spectra of pentacene films on Si wafers coated with 30 nm Al_2O_3: (a) Variation of deposition rate at a constant layer thickness of 20 nm and (b) variation of layer thickness at a constant deposition rate of 1.5 Å/s.

The noticeable peak near 5.6° in these spectra was identified to be the Bragg peak of pentacene's thin film phase (001) [322], while smaller peaks originate from the underlying substrates and are identical for all samples. As is visible in figure A.1 (a), a variation in deposition rate has no effect on pentacene's Bragg peak, indicating that the crystallinity of the pentacene film is unaffected by the deposition rate. For the case of a layer thickness variation, the Bragg peak's intensity increases for increasing layer thickness due to stronger reflections from the increased amount of material (see figure A.1 (b)). One may further observe that the width of the peak decreases slightly for thicker films, indicating slightly higher crystalline order in the thin film phase. A clear onset of the bulk phase peak can not be observed here as the pentacene layer is still too thin to make this peak visible [322].

B. ADDITIONAL SIMULATION DATA

The VOFET simulation data provided by Dr. Duy Hai Doan from WIAS has been analysed in chapter 6. This data was originally provided in complex file structures which are unsuitable for direct plotting in standard graphing software such as Gnuplot or Origin. Using a script written by Felix Kaschura (IAPP), it is possible to extract line profiles in the horizontal x-direction or vertical y-direction for any given variable for which the WIAS simulation provides data. In this manner, line profiles of the charge carrier density and electric potential distribution were extracted for different gate bias conditions in the simulated VOFET geometry with a 50 nm source insulator overlap.

In addition to the data shown in chapter 6, horizontal line profiles were obtained also at the positions $y = 60$ nm and $y = 125$ nm. These correspond to vertical positions inside the source electrode and just underneath the drain electrode (see figure B.1). Vertical line profiles were extracted at the positions $x = 1030$ nm and $x = 1100$ nm, i.e. just inside the insulator overlap region and in the vertical channel (see figure B.1).

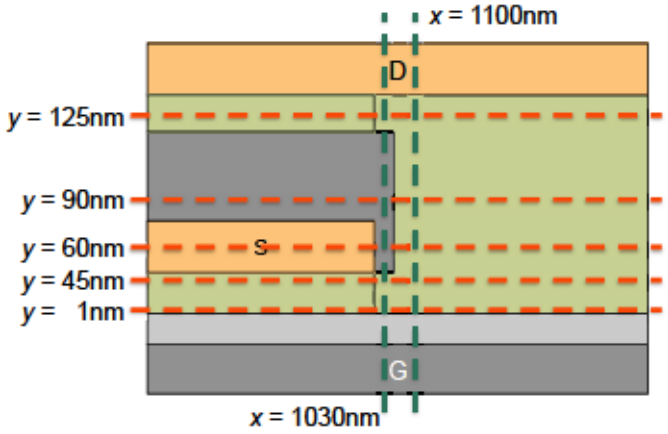


Figure B.1.: Schematic representation of the simulated VOFET geometry with a 50 nm-wide source insulator overlap discussed in chapter 6. Dashed red lines indicate the positions at which horizontal line profiles have been extracted. Dashed dark green lines indicate the positions at which vertical line profiles have been extracted. The extracted line profiles for different gate bias conditions are shown in figures 6.6, 6.7, 6.10 and B.2 to B.5.

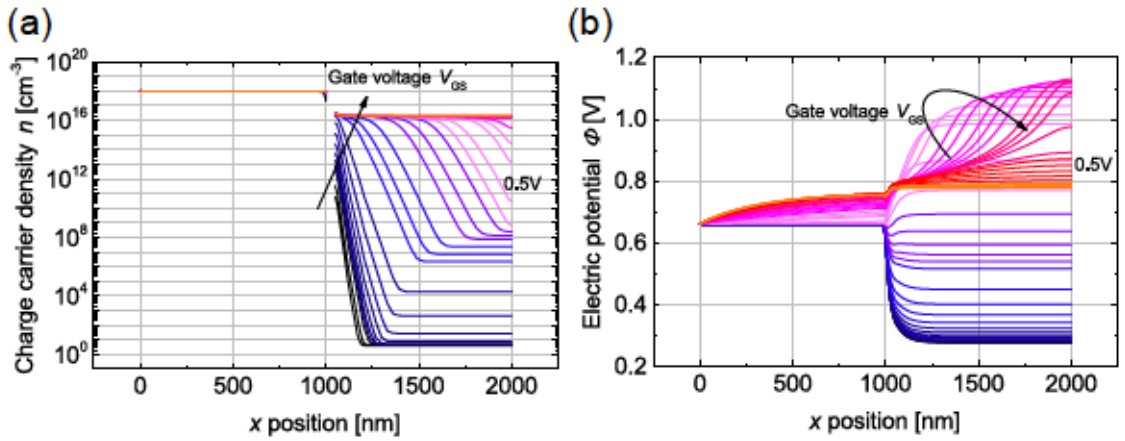


Figure B.2.: Lateral charge carrier density (a) and electric potential (b) profiles in the bottom semiconductor layer of a VOFET with a small insulator overlap at a position $y = 60$ nm, i.e. 10 nm above the bottom edge of the source electrode. Blue lines indicate low V_{GS} and red indicates high V_{GS}.

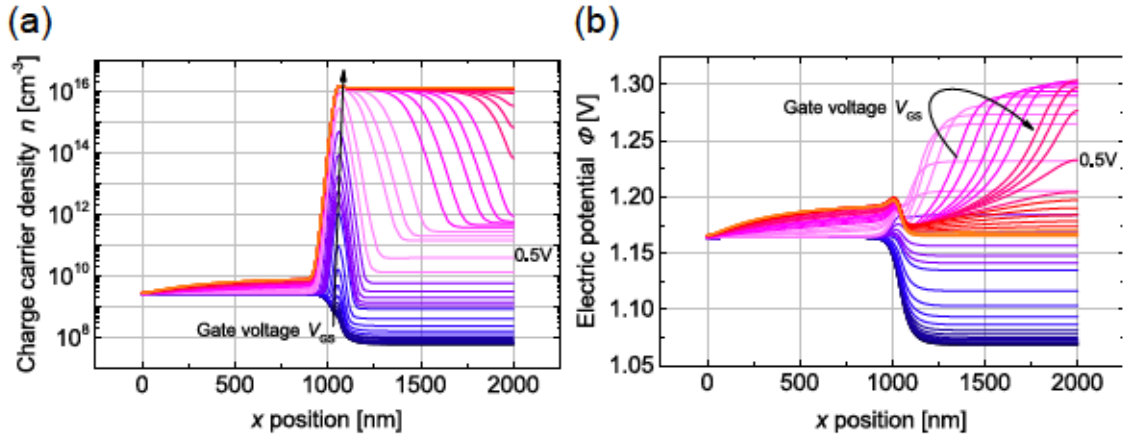


Figure B.3.: Lateral charge carrier density (a) and electric potential (b) profiles in the bottom semiconductor layer of a VOFET with a small insulator overlap at a position $y = 125$ nm, i.e. 25 nm below the bottom edge of the drain electrode. Blue lines indicate low V_{GS} and red indicates high V_{GS}.

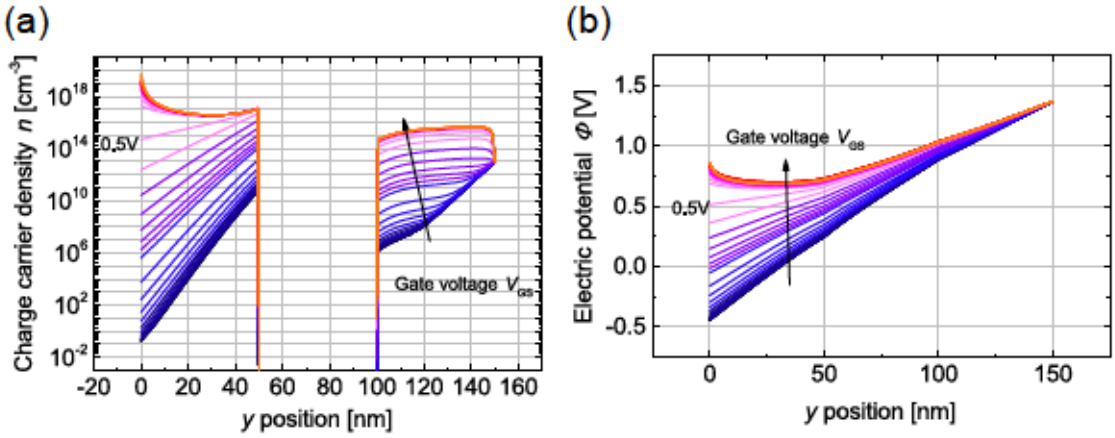


Figure B.4.: Vertical charge carrier density (a) and electric potential (b) profiles in the vertical channel region of a VOFET with a small insulator overlap at a position x = 1030 nm, i.e. 30 nm away from the vertical source edge, but still inside the insulator overlap region. Blue lines indicate low V_{GS} and red indicates high V_{GS}.

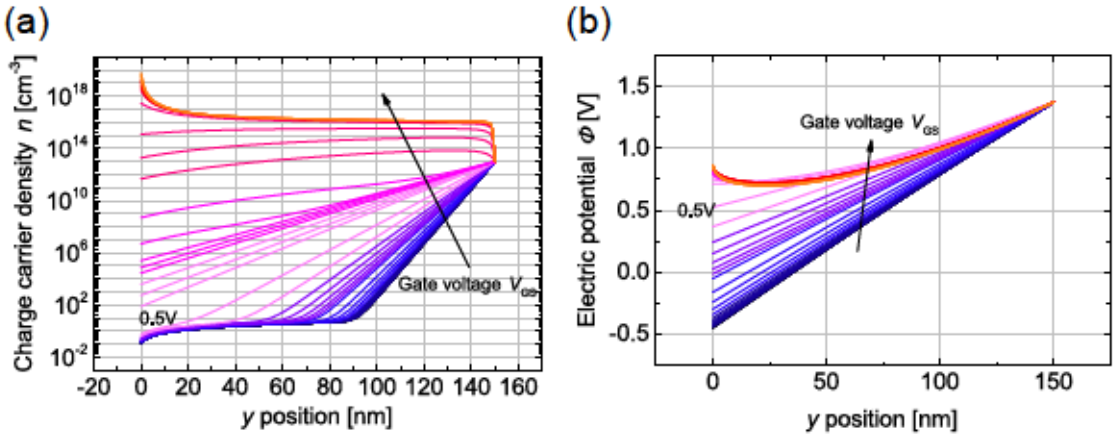


Figure B.5.: Vertical charge carrier density (a) and electric potential (b) profiles in the vertical channel region of a VOFET with a small insulator overlap at a position x = 1100 nm, i.e. 50 nm away from the vertical insulator edge. Blue lines indicate low V_{GS} and red indicates high V_{GS}.

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IMPORTANT SYMBOLS, CONSTANTS AND ABBREVIATIONS

SYMBOLS

Symbol	Quantity
A	Area
a	Lattice constant
c	Doping concentration
C_{diel}	Dielectric capacitance per unit area
d	Layer thickness
E	Energy
E_F	Fermi level
F	Electric field strength
f	Frequency
f_T	Cutoff frequency
g_m	Transconductance
$\hat{H}$	Hamiltonian operator
I	Electric current
I_D	Drain current
I_G	Gate current
j	Current density
L	Channel length
L_C	Contact overlap length
L_T	Transfer length
m^*	Effective mass of the electron
n	Charge carrier density
N_{it}	Density of interface traps
r	Deposition rate
$\vec{r}$	Position vector of electron
$\vec{R}_A$	Position vector of atom
R_C	Contact resistance
r_C	Specific contact resistance per unit area
R_{Ch}	Channel resistance
r_{Ch}	Specific channel resistance per unit area
R_{OFET}	OFET resistance
R_{Sheet}	Sheet resistance
S	Subthreshold swing
T	Temperature

Symbol	Quantity
V	Voltage
V_{GS}	Gate-source voltage
V_{DS}	Drain-source voltage
V_{th}	Threshold voltage
W	Channel width
Z	Impedance
ε_r	Relative permittivity
μ	Charge carrier mobility
ρ	Density
σ	Electrical conductivity
Φ	(el.) Potential
Φ_B	Energy barrier
Ψ	Electron wave function
ω	Angular frequency

PHYSICAL CONSTANTS

Quantity	Symbol	Value	Units
Elementary charge	e	1.60218×10^{-19}	C
Electron-volt energy	eV	1.60218×10^{-19}	J
Boltzmann's constant	k_B	1.38066×10^{-23}	JK^{-1}
Planck's constant	h	$6.62606957 \times 10^{-34}$	Js
Permittivity of free space	ε_0	8.85418×10^{-14}	Fcm^{-1}

ABBREVIATIONS

Abbrevation	Meaning
AFM	Atomic force microscopy
ALD	Atomic layer deposition
EDX	Energy-dispersive x-ray spectroscopy
EGDM	Extended Gaussian disorder model
HOMO	Highest occupied molecular orbital
LUMO	Lowest unoccupied molecular orbital
m-i-m	Metal-insulator-metal stack
m-i-s	Metal-insulator-semiconductor stack
OFET	Organic field-effect transistor
OPBT	Organic permeable base transistor
OSBT	Organic Schottky barrier transistor
OSIT	Organic static induction transistor
p-i-p	p-doped - intrinsic - p-doped stack
POEM	Electric potential mapping via thickness variation
TLM	Transmission line method
UPS	Ultraviolet photon spectroscopy
VOFET	Vertical organic field-effect transistor

LIST OF FIGURES

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Hiermit versichere ich, dass ich die vorliegende Arbeit ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt habe. Die aus fremden Quellen direkt oder indirekt übernommenen Gedanken sind als solche kenntlich gemacht. Die Arbeit wurde bisher weder im Inland noch im Ausland in gleicher oder ähnlicher Form einer anderen Prüfungsbehörde vorgelegt. Weiterhin versichere ich, dass keine früheren Promotionsverfahren stattgefunden haben.

Ich erkenne die Promotionsordnung der Fakultät Mathematik und Naturwissenschaften an der Technischen Universität Dresden vom 23.02.2011 an.

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Dresden, den 29.03.2016